Sierra 1914B

DATA TRANSMISSION TEST SET

OPERATION/MAINTENANCE MANUAL

SMM-1914B

ISSUE 1

PHILCO Ford

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NOTICE
TO THE PURCHASER OF
THE SIERRA 1914B DATA TRANSMISSION TEST SET

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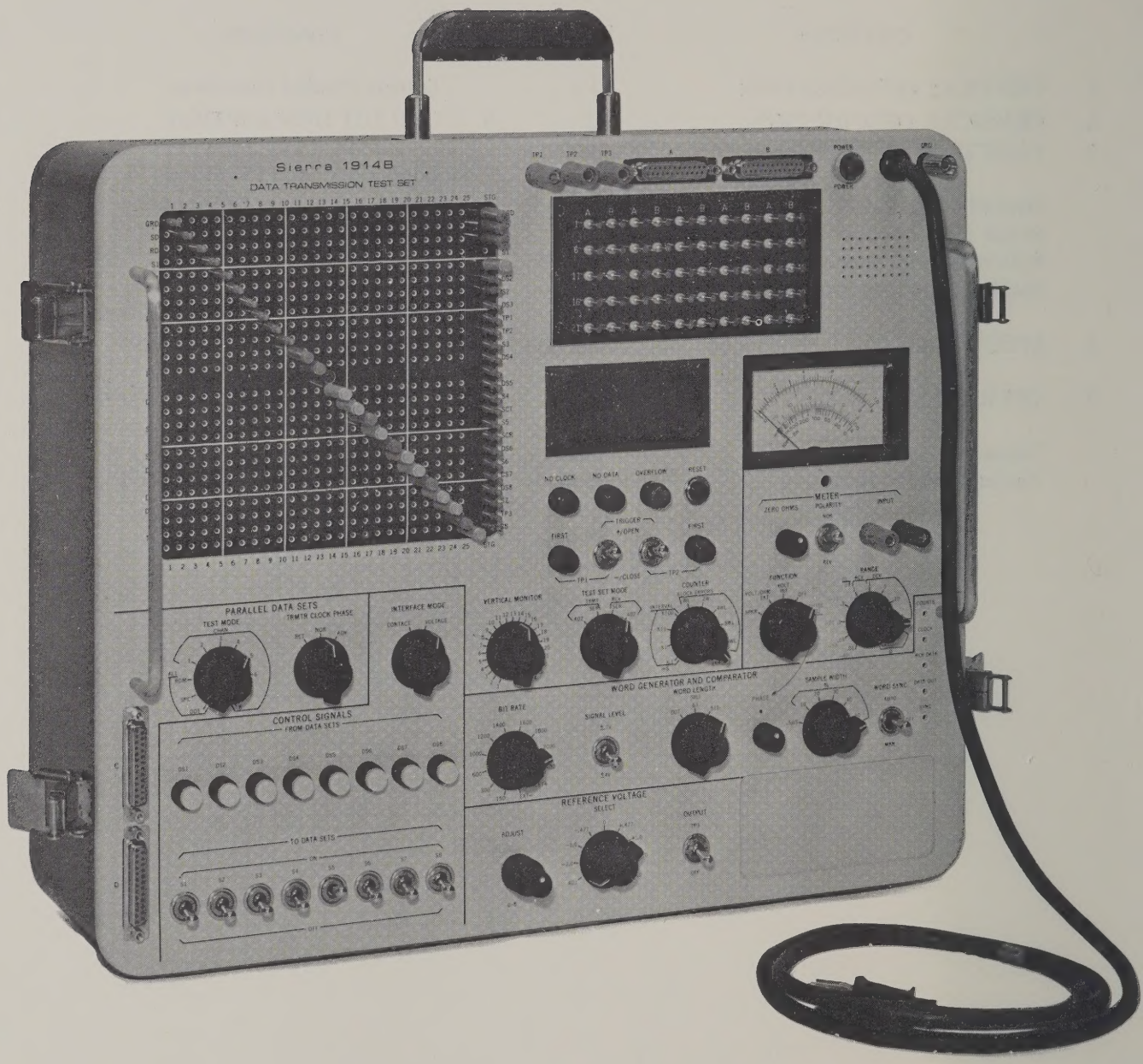


Figure 1-1. Sierra 1914B Data Transmission Test Set

SECTION 1
GENERAL INFORMATION

1.01 This maintanance manual describes the Sierra 1914B and provides operation and maintenance instructions. Circuit descriptions, simplified-circuit diagrams, and functional schematics are included along with detailed-circuit schematics. A list of replaceable parts and reference information are also provided in this manual.

1.02 The Sierra 1914B Data Transmission Test Set is a portable instrument for tests of voiceband data systems. It is compatible with digital and analog modems now in operation and contains built-in flexibility to allow its use on future systems. Either synchronous or asynchronous serial-data modems can be tested. For tests of asynchronous modems, an internal clock produces test messages at any of ten bit rates selected. Synchronous-data modems that recover their own clock signals can be tested at any bit rate in the range of 10 to 20,000 bits per second, as determined by modem characteristics. Two detectors and associated lamps provide a visual indication of a failure of the clock signal and a failure of the data signal. Control signals applied to the interface of the modem are generated by individual switches. Control signals from the modem are readily monitored by indicator lamps.

1.03 The 1914B can be used at both the transmitting and receiving station of a data system. A major advantage of the 1914B is its programmable crosspoint matrix, which establishes the connection of the internal test circuits to the interface leads of the data modem. This matrix provides total flexibility in all interface interconnections and, together with an array of interface switches, permits tests of a modem or data system while the data terminal is connected to the transmitting or receiving modem.

1.04 The performance of the data transmission system is evaluated in terms of the bit or block error rate of the system. The errors are tabulated and displayed on an electronic decade counter. In block error tests the block length can be adjusted from a minimum of 63 to a maximum in excess of 8000 bits. In tests of asynchronous modems the received data signal is sampled at the midbit position by a pulse which is adjustable in width. This feature permits determining in one test the error rate of the system and also the margin against errors.

1.05 Features of the 1914B are:

- Full compatibility with most voice-frequency modems
- Performs dynamic and static tests of data transmission systems
- Tests both asynchronous and synchronous serial modems as well as eight-channel parallel modems
- Bit and block error counting
- Three types of digital test messages – dot signal, 63-bit, and 511-bit pseudorandom word
- Checks sequence of control signals and measures time intervals
- Provides internally clocked bit rates for tests of asynchronous modems in the range of 150 to 2400 bits per second
- Can be operated from clock signal of synchronous modems at bit rates in the range of 10 to 20,000 bits per second.
- Automatic and manual word synchronization
- Variable-width sample window for receive data bits to permit determining error rate margins
- Internal dc voltmeter for checks of dc interface voltages
- High-impedance ac voltmeter and loudspeaker amplifier for monitoring line signals
- Interface signals conform to EIA specification RS 232B and CCITT recommendations
- Compatible with Bell System 902-903 series test sets
- Equivalent to Western Electric Company Model 914B data test set.

SECTION 2
PHYSICAL DESCRIPTION

2.01 The 1914B Data Transmission Test Set is contained in a carrying case measuring approximately 18-1/2 inches in width, 15 inches in height, and 7-1/2 inches in depth. It weighs about 27 pounds. Figure 1-1 shows the 1914B ready for use, Figure 2-1 shows the test set with its cover in place, and Figure 2-2 is a view of the inside of the cover showing the two interface connector cables, the two test leads, and the 4-dB attenuator.

Figure 2-1. Sierra 1914B with Cover in Place

2.02 The test set is powered by a self-contained power supply which draws approximately 60 watts of 105- to 125-volt, 48- to 65-Hz commercial power. It will operate efficiently in an environment with an ambient temperature ranging from +40° to +120°F and a relative humidity of from 20 to 95 percent.

2.03 Figures 2-3 and 2-4 show the front panel of the 1914B. The program matrix in the upper left-hand corner provides access to the interface leads of the data set being tested. The 25 vertical buses connect to the interface leads and the 24 horizontal buses connect to the test circuits provided by the 1914B. Connections from the input or output leads of the test circuits to the interface leads are made by inserting program pins at the intersections of the appropriate vertical and horizontal buses of the matrix. The meanings of the designations stamped alongside the buses are given in the following tabulation.

1914B Designation	EIA RS232B or C Designation	CCITT V-24 Designation	Meaning
GRD	AA,AB	101, 102	Ground
SD	BA	103	Send Data, Output
RD	BB	104	Receive Data, Input
SCT	DB	114	Serial Clock Transmit, Input
SCR	DD	115	Serial Clock Receive, Input
DSI-DS8			Inputs to Lamps DS1-DS8
S1-S8			Outputs from S1-S8
TP1-TP3			Test Point Connections
STG			Program Pin Storage

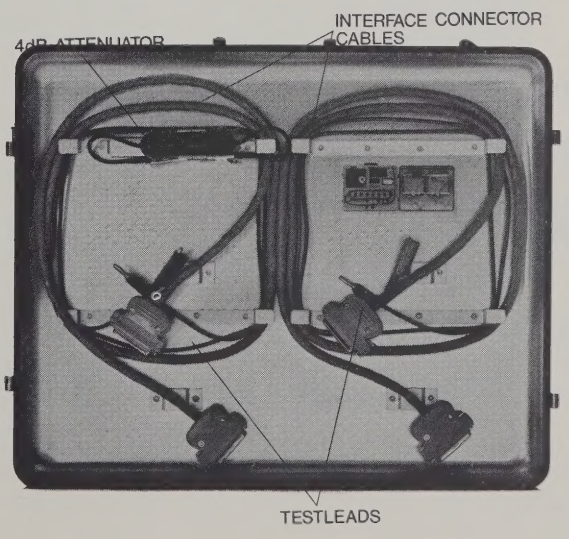


Figure 2-2. Inside Front Cover

2.04 The interface leads connect through push-pull selector switches on the front panel (Figure 2-3) to the vertical buses of the program matrix. These switches permit testing a data set on an in-service basis in either a bridging or terminating mode. They also offer a means of testing data sets having more than 25 interface leads.

2.05 The other front-panel controls, indicators, and connectors are described in Table 2-1. Abbreviations marked on some of the switch positions are defined as follows:

Designation	Meaning
CHAN	Parallel Data Channel
ALL RDM	Random Test Signal on All Channels
ALL SPC	Spacing Signal on All Channels
ALL DOT	Dot Signal on All Channels
SER	Serial
WL, 2WL, etc.	Word Length; Block Length in Multiples of the Word Length (63 or 511) Selected
AUTO	Automatic
MAN	Manual

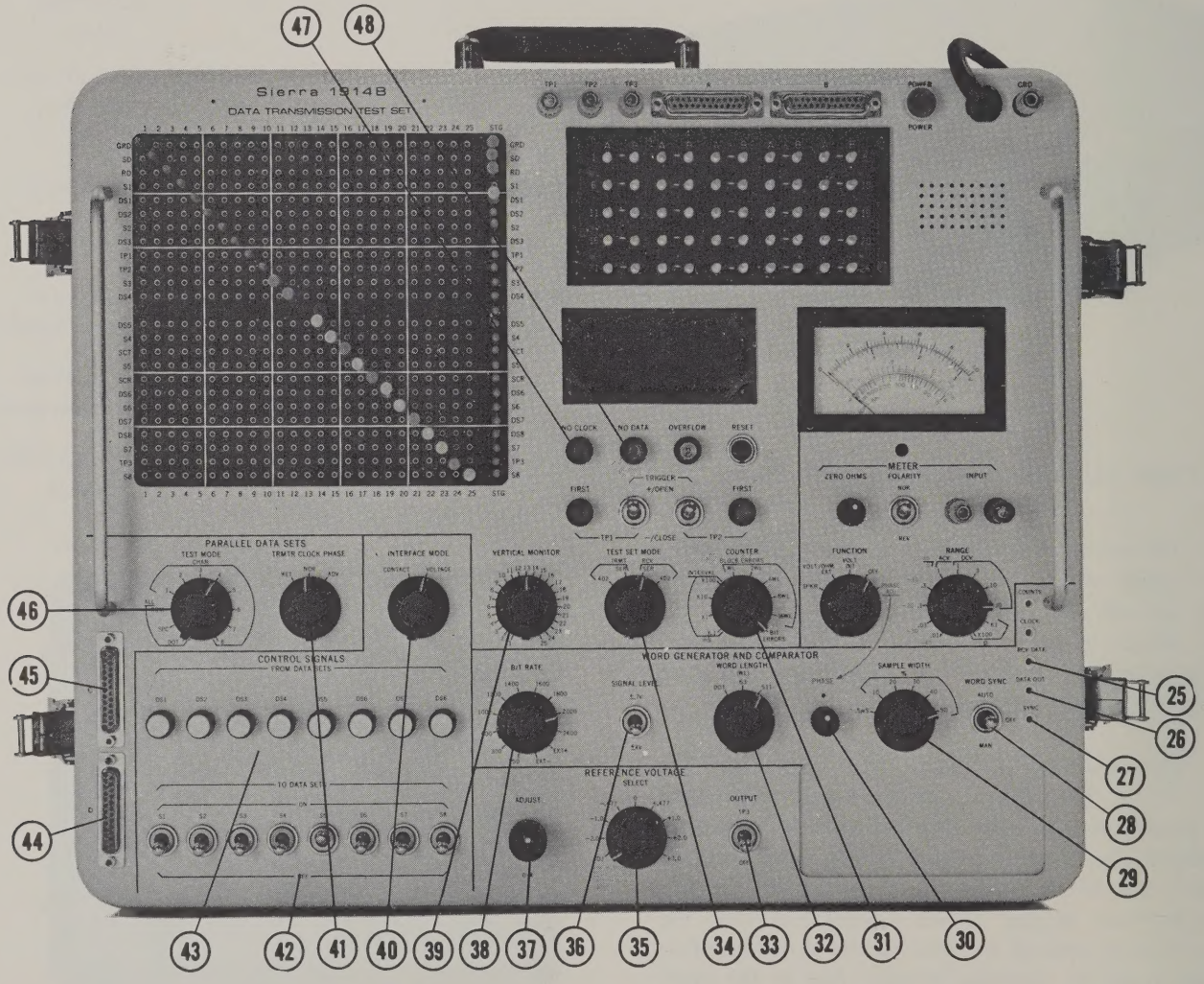


Figure 2-3. Sierra 1914B Data Transmision Test Set, Front Panel

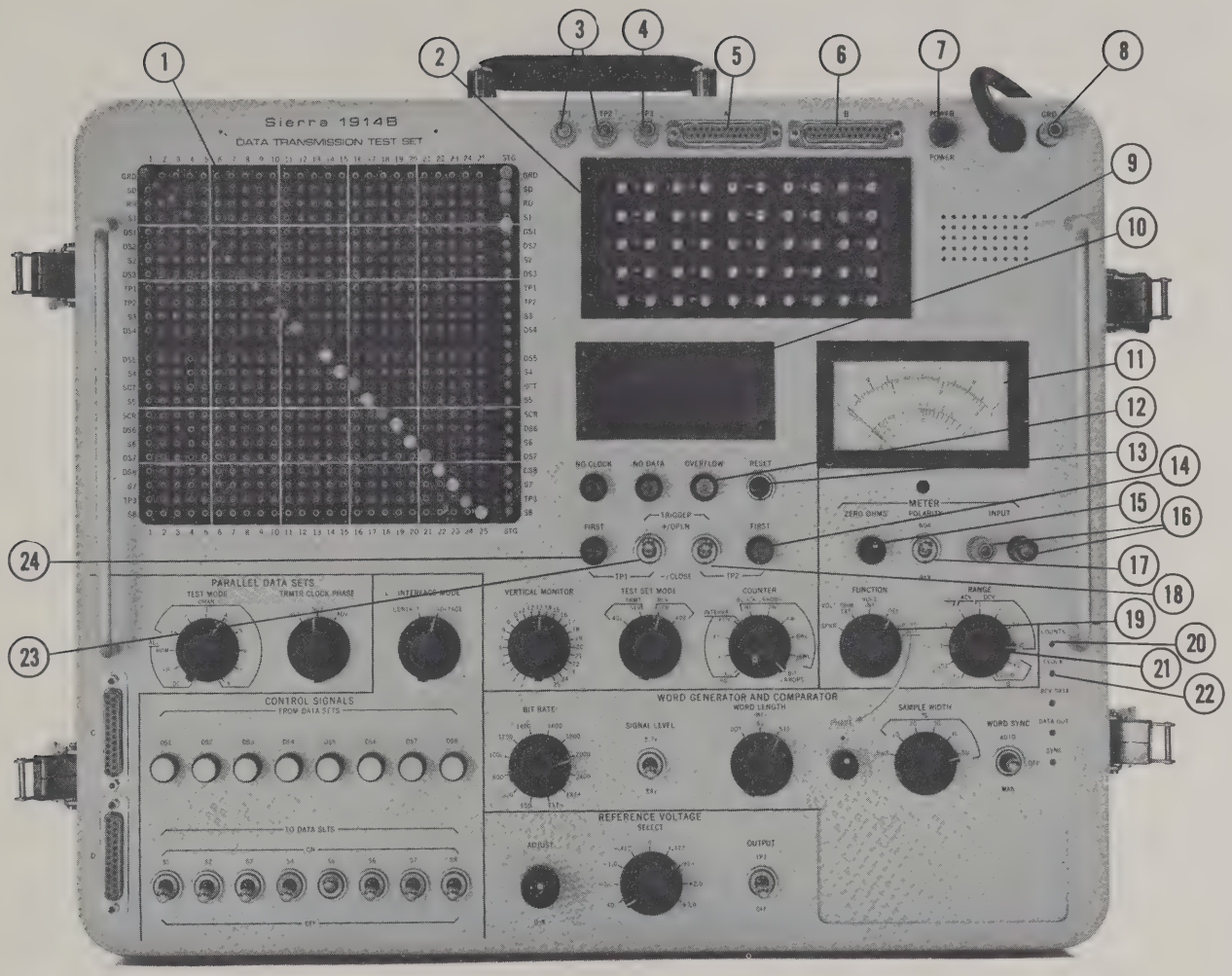


Figure 2-4. Sierra 1914B Data Transmission Test Set, Front Panel

Table 2-1. Front-Panel Controls, Indicators, and Connectors

INDEX (FIGURES 2-3 & 2-4)	DEVICE	FUNCTION
1	Program Matrix	Provides access to the interface leads of the data set being tested.
2	Interface selector switches	Provide access to the interface leads for in-service testing of data sets.
3	TP1 and TP2 test points	Provide means of introducing signals into the interval counter. Also provide access to TP1 and TP2 matrix buses.
4	TP3 test point	Provides access to the TP3 matrix bus and the selected reference voltage, when the REFERENCE VOLTAGE OUTPUT switch is in the TP3 position.
5	Connector A	Provides connection to serial data set interface.

Table 2-1. Front-Panel Controls, Indicators, and Connectors (Cont)

INDEX (FIGURES 2-3 & 2-4)	DEVICE	FUNCTION
6	Connector B	Provides connection to business machine interface for in-service tests of serial data sets.
7	POWER switch and lamp	Provides means of turning set on and off and provides power on indication.
8	GRD connector	Provides means of connecting an external ground.
9	Loudspeaker	Permits the operator to audibly monitor signals on any line connected to the METER INPUT terminals when the FUNCTION switch is in the SPKR position.
10	Counter display	Provides a two-digit readout of error count or interval, depending on the position of the COUNTER switch.
11	METER	Indicates ac voltage, dc voltage, or resistance, depending on the setting of the FUNCTION and RANGE switches.
12	OVERFLOW lamp	When lighted, indicates counter capacity has been exceeded.
13	RESET switch	Clears counter and resets interval test circuits.
14	FIRST TP2 lamp	When lighted, indicates preselected signal appeared first on TP2 lead.
15	ZERO OHMS adjustment	Provides a means of calibrating the ohmmeter for zero ohms.
16	INPUT connectors	Provide a means to connect the speaker and the meter to an external source. The voltage applied to the red connector should be positive with respect to the voltage at the black connector when the POLARITY switch is in the NOR position.
17	POLARITY switch	Provides a means to reverse the polarity of the dc meter.
18	TP2 TRIGGER switch	Selects TP2 triggering mode.
19	FUNCTION switch	Switches the meter circuit for the desired meter use.
20	COUNTS test point	Delivers a signal consisting of a pulse for every 100 errors recorded on the internal counter.
21	RANGE switch	Switches the meter to the desired operating range. Adjusts speaker volume when the FUNCTION switch is in the SPKR position.
22	CLOCK test point	Delivers a signal consisting of a 4.5-volt square wave with the same frequency as the test set bit rate.
23	TP1 TRIGGER switch	Selects TP1 triggering mode.
24	FIRST TP1 lamp	When lighted, indicates preselected signal appeared first on TP1 lead.
25	RCV DATA test point	Delivers the data signal from the RD horizontal bus of the matrix, when the test set is in the serial receiver mode.
26	DATA OUT test point	Delivers the bipolar data signal produced by the word generator.
27	SYNC test point	Delivers the positive word-sync signal.
28	WORD SYNC switch	Selects either manual or automatic word synchronization.
29	SAMPLE WIDTH switch	Selects width of sample pulse.
30	PHASE adjustment	Used for fine adjustment of the bit synchronization circuits.

Table 2-1. Front-Panel Controls, Indicators, and Connectors (Cont)

INDEX (FIGURES 2-3 & 2-4)	DEVICE	FUNCTION
31	COUNTER switch	Permits measurement of block error rate, bit error rate, or interval.
32	WORD LENGTH switch	Selects dot, 63-bit, or 511-bit test word.
33	OUTPUT switch	When in the TP3 position, delivers the selected reference voltage to test point TP3 and to the TP3 horizontal bus of the matrix.
34	TEST SET MODE switch	Provides the appropriate test mode for the data set under test.
35	SELECT switch	Enables selection of a reference voltage.
36	SIGNAL LEVEL switch	Selects either ±0.7 or ±4 volts for SD output level.
37	ADJUST control	Used for coarse and fine adjustment of the reference voltage when the SELECT switch is in the ADJ position.
38	BIT RATE switch	Sets rate of timing signal used to drive word generator and comparator.
39	VERTICAL MONITOR switch	Provides a means of connecting the dc voltmeter to any of the interface leads of the data set.
40	INTERFACE MODE switch	Selects contact or voltage mode for control signals.
41	TRMTR CLOCK PHASE switch	Sets phase relationship of clock and parallel data signals.
42	S1-S8 switches	Apply control signals to the correspondingly numbered horizontal buses on the matrix.
43	DS1 to DS8 lamps	When lighted, indicate presence of control signals on the correspondingly numbered horizontal buses of the matrix.
44	Connector D	Provides connection to receiving 402-type data sets.
45	Connector C	Provides connection to transmitting 402-type data sets.
46	TEST MODE switch	Provides a means of applying the desired test signal to the parallel data channels.
47	NO CLOCK lamp	When lighted, indicates absence of clock signals.
48	NO DATA lamp	When lighted, indicates absence of data signal.

SECTION 3
FUNCTIONAL DESCRIPTION

3.01 The functional description of the 1914B is presented in four parts – overall function, serial transmit and receive functions, parallel data transmit function, and parallel data receive function.

Overall Function (Figure 3-1)

3.02 The program matrix provides the means for connecting the data set interface leads to the 1914B test circuits in the desired manner. The matrix consists of 24 horizontal and 25 vertical buses. The vertical buses connect through selector switches and connector A or B to the interface leads of the data set being tested. The horizontal buses connect to the various 1914B test circuits. Connection between a vertical bus and a horizontal bus is made by a pin inserted in the matrix. When series resistance is to be inserted at the connection, special pins with built-in resistors are used. Each of the 25 interface leads is shunted by a 300-kilohm resistor to provide marginal open-circuit loading for contact interfaces. Table 3-1 describes the test signals available at each of the horizontal buses of the matrix.

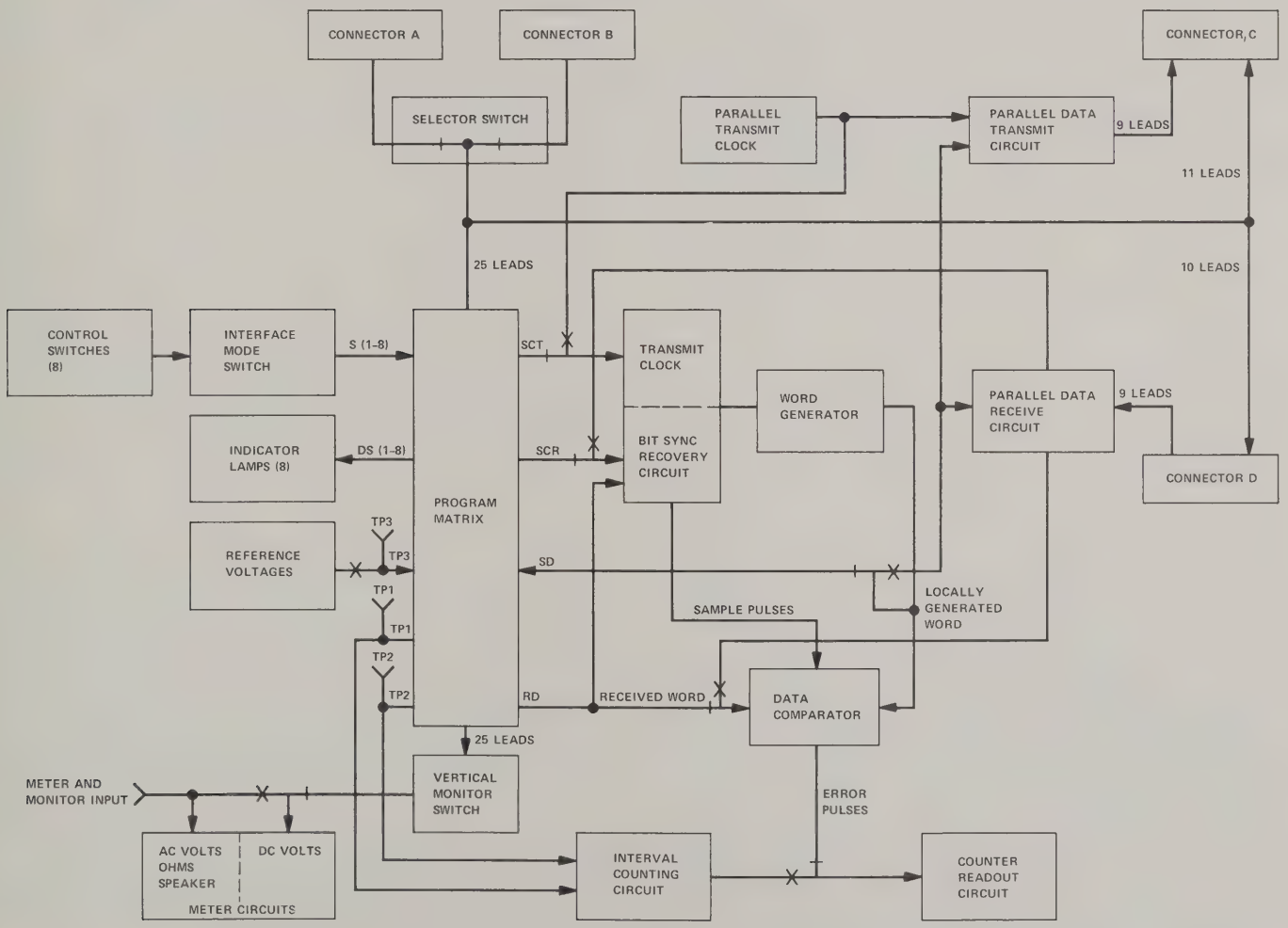


Figure 3-1. Overall Functional Block Diagram

Table 3-1. Signals Available on Program Matrix Horizontal Buses

HORIZONTAL BUS	SIGNAL
GRD	Test ground.
SD	Send Data signals when the TEST SET MODE switch is in the TRMT position.
RD	Receive Data signals when the TEST SET MODE switch is in the RCV position.
S1-S8	Control signal from the test set, present when the corresponding front-panel switch S1-S8 is the ON position. The signal is either a ±-voltage level or a contact closure, depending on the position of the INTERFACE MODE switch.
DS1-DS8	Control signal from the data set. When present corresponding front-panel lamp DS1-DS8 is lit. With the INTERFACE MODE switch in the CONTACT position, a contact closure to ground on a horizontal bus lights the corresponding indicator lamp. When the INTERFACE MODE switch is in the VOLTAGE position, a +4-volt signal present on a horizontal bus activates the lamp driver, which in turn lights the corresponding lamp.
TP1, TP2	Inputs to the test set interval counting circuit. These buses are also connected to front-panel test jacks TP1 and TP2, respectively, and may be used for connecting external signals to these matrix buses when the COUNTER switch is in any of the ERRORS positions.
SCT	Transmit clock signal.
SCR	Receive clock signal.
TP3	The signal applied to front-panel test jack TP3 when the OUTPUT switch is in the OFF position; or, when the OUTPUT switch is in the TP3 position, the reference voltage selected by the SELECT switch.

3.03 Each of the 25 interface selector switches has an A section and a B section, corresponding to interface connectors A and B. The switches are normally closed, and must be opened for additional functions. When both sections of a switch are closed, the corresponding pins of connectors A and B are interconnected. The latter mode of operation is useful when, for example, a business machine is connected to connector B and the data set is connected to connector A to provide a setup for in-service testing. By closing both the A and B sections of an interface selector switch, the signal on that particular lead becomes available on a vertical bus of the program matrix in a bridging connection. Any lead between the terminal and the data set can also be opened for testing the signals at either the terminal or data set by opening or closing the A or B section of the appropriate interface selector switch.

3.04 The meter circuits permit the operator to measure dc voltage, ac voltage, resistance, and signal level in dBm (600-ohm line calibration). When ac volts or ohms are to be measured, the circuit to be measured must be connected to the METER INPUT terminals. An audio signal on a line connected to the METER INPUT terminals can be monitored on the built-in loudspeaker by turning the FUNCTION switch to the SPKR position.

3.05 The VERTICAL MONITOR switch can be used to select a vertical matrix bus whose dc voltage is to be measured, or the dc voltage to be measured can be applied to the METER INPUT terminals.

3.06 The interval counting circuit measures the time interval between a signal on the TP1 bus and

another signal on the TP2 bus (or test jacks TP1, TP2), and drives the front-panel digital display to indicate the interval in milliseconds or multiples thereof. The signal can be a positive or negative transition or a contact opening or closing, depending on the position of the TRIGGER switches. The signals can be applied to the counting circuit either from the matrix or from the front-panel TP1 and TP2 jacks. The interval counting circuit also determines which signal arrives first and indicates this information by means of the TP1 FIRST or TP2 FIRST lamp.

3.07 The reference voltage circuit provides fixed voltages of ±0.477, ±1, ±2, and +7 volts, and an adjustable voltage of 0 to +8 volts. The desired voltage is selected by the REFERENCE VOLTAGE SELECT switch and is delivered to the front-panel TP3 jack and the TP3 matrix bus when the OUTPUT switch is in the TP3 position.

3.08 A power supply in the 1914B provides two unregulated outputs of +23 and +200 volts and three regulated outputs of +12, -12, and +5 volts for operation of all of the test set circuits. Input to the power supply is 105 to 125V, 48 to 65 Hz.

Serial Transmit and Receive Function (Figure 3-2)

3.09 The same clock circuit is used in both the transmit and receive modes. The clock rate is set by the front-panel BIT RATE switch. When this switch is in either of the EXT positions, the timing signal present on the SCT or SCR bus will drive the test set. In testing receiving asynchronous data sets, the clock circuits recover the bit timing signal from the incoming received data stream. The bit synchronization recovery circuit, therefore, controls the clock rate in the receive mode; the PHASE control permits precise synchronization with the incoming data signal.

3.10 The clock signal, either internal or external, is applied to the word generator, which generates a dot signal (alternate marks and spaces), 63-bit test words, or 511-bit test words, depending on the setting of the WORD LENGTH switch.

3.11 Errors in the received data signal are detected by comparing it with a test signal that is identical to the transmitted test signal. The comparison requires that the received and the locally generated test signals be synchronized, i.e., that the corresponding bits of the two test signals be aligned. Word synchronization is accomplished either manually or automatically, depending on the setting or the WORD SYNC switch.

3.12 When the WORD SYNC switch is momentarily depressed to the MAN position, the receiving test signal generator is forced into synchronism with the received test signal within a small fraction of a second. When the WORD SYNC switch is set to the AUTO position, the receiving test signal generator is continuously resynchronized with the received test signal. Because of the method of synchronization, the error count recorded in the AUTO mode is approximately three times the true error count.

3.13 The received data signal is compared with the locally generated test signal only during a short sampling interval coincident with the center of each received bit. In tests of asynchronous data sets, the sampling interval can be lengthened to include greater portions of the bit. Any discrepancy between the received bit and the locally generated bit during the sampling interval is registered as an error. The SAMPLE WIDTH switch selects the width of the sample interval in steps of 10 percent of the bit interval up to a maximum of 50 percent. This variable-width sampling technique allows checking the error margin of the received signal.

3.14 With the COUNTER switch set to the BIT ERRORS position individual bits in error are counted. When the COUNTER switch is set to one of the BLOCK ERRORS positions, the number of blocks of the selected length that contain one or more errors is counted. The block length is selected as the indicated multiple (i.e., WL, 2WL, etc.) of the word length (i.e., 63 or 511). The minimum block length is 63 bits, the maximum is in excess of 8000 (16 x 511) bits.

Parallel Data Transmit Circuits (Figure 3-3)

3.15 The dot generator, driven by the 75-Hz parallel transmit clock multivibrator, produces a 75-bps dotting signal. In the ALL DOT position of the TEST MODE switch, this signal is applied through output drivers and connector C to the eight parallel data channels. The output drivers provide the contact closure type of interface required by parallel data sets. The control leads of the data set appear on the matrix.

3.16 In the ALL RDM position of the TEST MODE switch, test words from the word generator are applied to all eight parallel data channels. In the ALL SPC position of the TEST MODE switch, a space signal is applied to the eight channels, while in any one of the CHAN positions of the switch, test words are applied to the selected channel and the dot signal is applied to the other channels.

3.17 The output of the dot generator is also applied to the timing channel of the parallel data set. By means of the TRMT CLOCK PHASE switch, this dot signal can be advanced or retarded in phase by 1.5 milliseconds

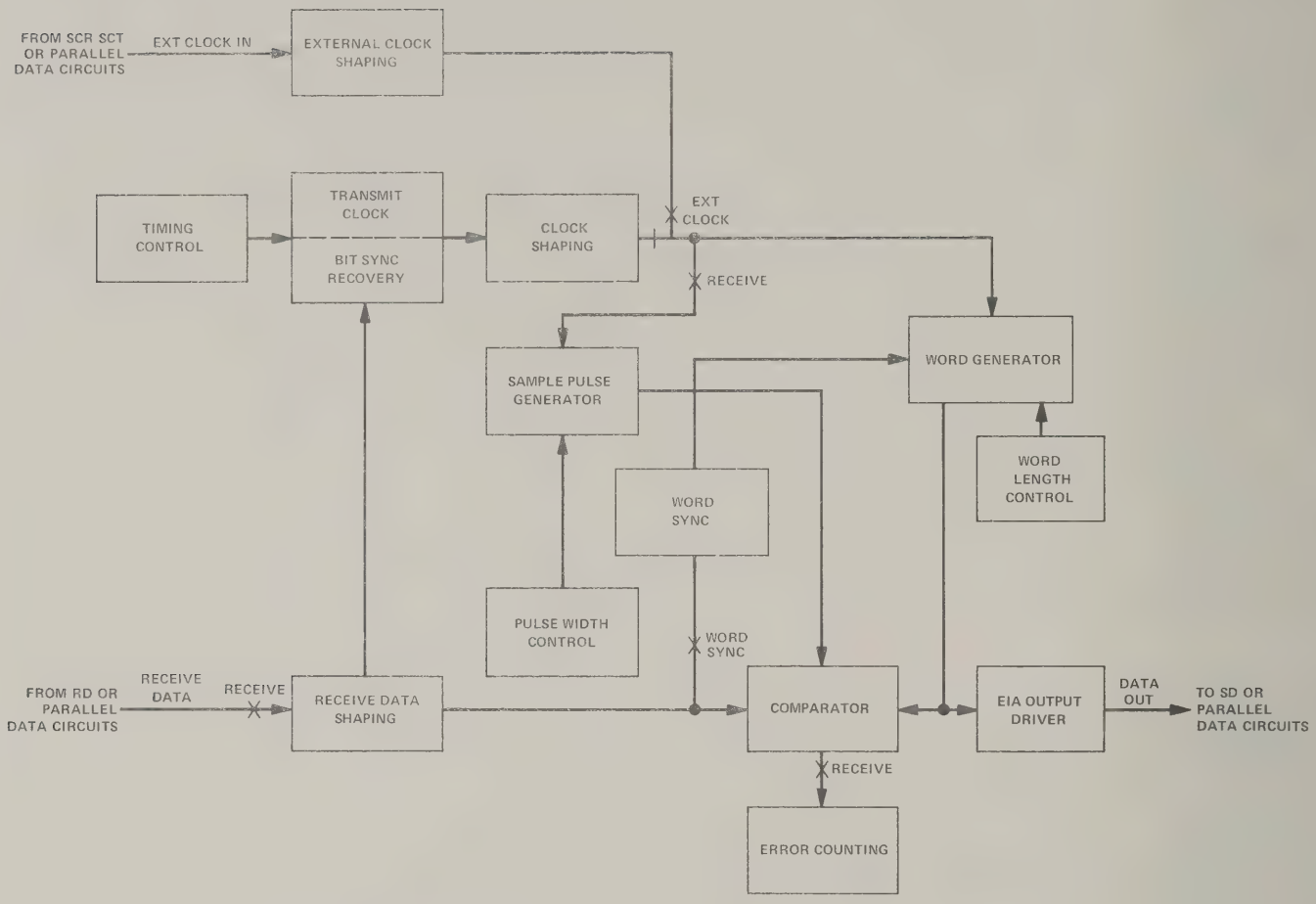


Figure 3-2. Serial Transmit and Receive Circuits

with respect to the data signal to simulate changes in phase relationship between the clock and data signals.

Parallel Data Receive Circuits (Figure 3-3)

3.18 Connections from the receiving parallel data set to the test set are made through connector D, the control leads again are connected to the matrix. If the data channels are to be tested individually, the TEST MODE switch is turned to the desired channel, and error checks are made in the same way as for serial data sets, as described in paragraphs 3.09 through 3.14.

3.19 If all channels are to be tested simultaneously, the TEST MODE switch is turned to ALL RDM. The combined output from all channels is compared to the output of the word generator. If any channels contain errors, the errors will be registered on the counter display.

3.20 The signal on the timing channel is applied through the level converter to the external clock input of the word generator and drives the word generator and comparator circuits.

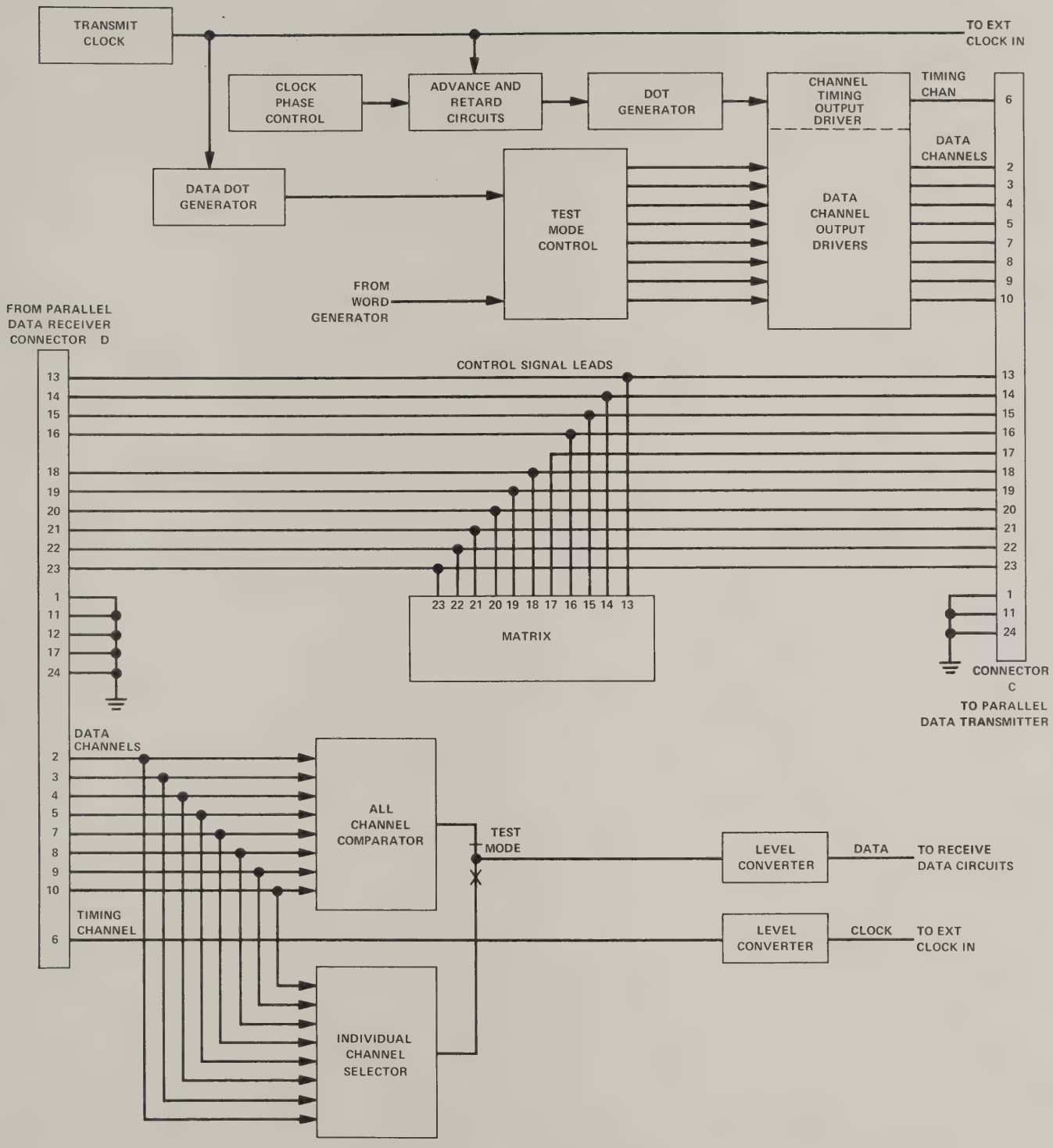


Figure 3-3. Parallel Transmit and Receive Circuits

SECTION 4
SPECIFICATIONS

4.01 The signal outputs of the 1914B are accessible at the program matrix and the various test points on the front panel. Table 4-1 lists the specifications.

Table 4-1. Specifications

Parameter	Characteristic
SD (Send Data)	Bipolar, NRZ (nonreturn to zero) signal, ±3.5 to ±5 volts or ±0.7 volt in amplitude from an impedance of 200 ohms with rise and fall times not exceeding 1 μsec.
S1-S8 Control Signals	±3.5 to ±5 volt dc levels in the voltage mode, contact closures to ground and open circuits in the contact mode.
Internal Clock Bit Rates	150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, and 2400 bits per second ±3%.
RD (Receive Data)	Bipolar, NRZ (nonreturn to zero) signal, minimum amplitude ±3 volts; input resistance 2400 ohms in series with a silicon diode junction.
SCR (Serial Clock; Receive)	Bipolar square wave, minimum amplitude ±3 volts; input resistance 2400 ohms in series with silicon diode junction.
SCT (Serial Clock; Transmit)	Same as SCR.
DS1-DS8 Voltage Mode	+3 dc level to light lamp; input resistance 3000 ohms in series with a silicon diode junction.
DS1-DS8 Contact Mode	Contact closure to ground to light lamp; lamp current 40 mA, lamp voltage +23 volts.
Received Bit Rates (Internal Clock)	150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, and 2400 bits per second ±5%.
Power Required	105–125 Vac, 48–65 Hz, approximately 60 watts.
Operating Temperature Range	+40° to +120°F
Dimensions	Width 18-1/2 inches, Height 15 inches, Depth 7-1/2 inches.
Weight	27 pounds (approximate).

SECTION 5
OPERATION

5.01 This section of the manual explains the operation of the matrix, the selector switches, the interval counter, the meter, and the loudspeaker, and it describes typical tests of serial data sets and analog data sets. For detailed operating instructions for a particular type of data set and for detailed test requirements, refer to local procedures or to the modem manufacturer's recommendations.

5.02 Carefully unpack and inspect each instrument for damage. If any evidence of damage is observed, contact:

Customer Service Department
Sierra Electronic Operation
Philco-Ford Corporation
3885 Bohannon Drive
Menlo Park, California 94025
Telephone (415) 322-7222

NOTE: Do not repackage damaged or faulty equipment for return to Sierra Electronic Operation under the provisions of the warranty without first contacting Sierra for specific instructions.

5.03 **Program Matrix:** The matrix, which provides a convenient means of interconnecting the data set interface leads with the test set circuits, is described in detail in Paragraph 3.02. Red pins provide a direct connection between the horizontal and vertical buses; gray pins and green pins make the interconnections through built-in 10-ohm and 18-ohm resistances, respectively. The resistors simulate cable resistance.

5.04 **Interface Selector Switches:** Figure 5-1 is a schematic diagram of the interface selector switches. The switches consist of an A and a B section, each of which is a combination switch and test point. This feature makes all interface signals accessible for external connections and also permits testing modems with the terminal equipment connected to the test set. By selectively closing and opening individual interface leads, signal flow between the modem and the terminal equipment can be checked by the test set in a bridging or terminating mode.

5.05 **Interval Counter:** The interval counter can be used to check the sequence in which control leads are actuated and the time delays involved can be measured. The counter is described in detail in Paragraph 3.06, and its use is described below.

5.06 To measure the interval between two signals, proceed as follows:

Step 1
Apply the signals to be measured either directly to TP1 and TP2, or to the TP1 and TP2 horizontal matrix buses by means of shorting pins.

Step 2
Set the TRIGGER TP1 switch depending on the expected TP1 signal and set the TRIGGER TP2 switch in accordance with anticipated signal on TP2.

Step 3
Set the COUNTER switch to the appropriate range for the interval to be measured, (msec X.1, X1, X10, or X100.)

Step 4
Set the BIT RATE switch to any internal bit rate.

Step 5
Set the TEST SET MODE switch to TRMT SER.

Step 6
Press the RESET switch momentarily to clear the counter.

Step 7
When the measurement takes place, the number in the counter display multiplied by the factor selected by the COUNTER switch will be the measured interval in milliseconds.

Step 8
If the FIRST TP1 lamp lights, it means that the signal on TP1 occurred before the signal on TP2; conversely, if the FIRST TP2 lamp lights, it means that the signal on TP2 occurred before the signal on TP1.

5.07 In addition to measuring the interval between two signals, pulse duration can be measured by applying the same signal to both the TP1 and TP2 leads.

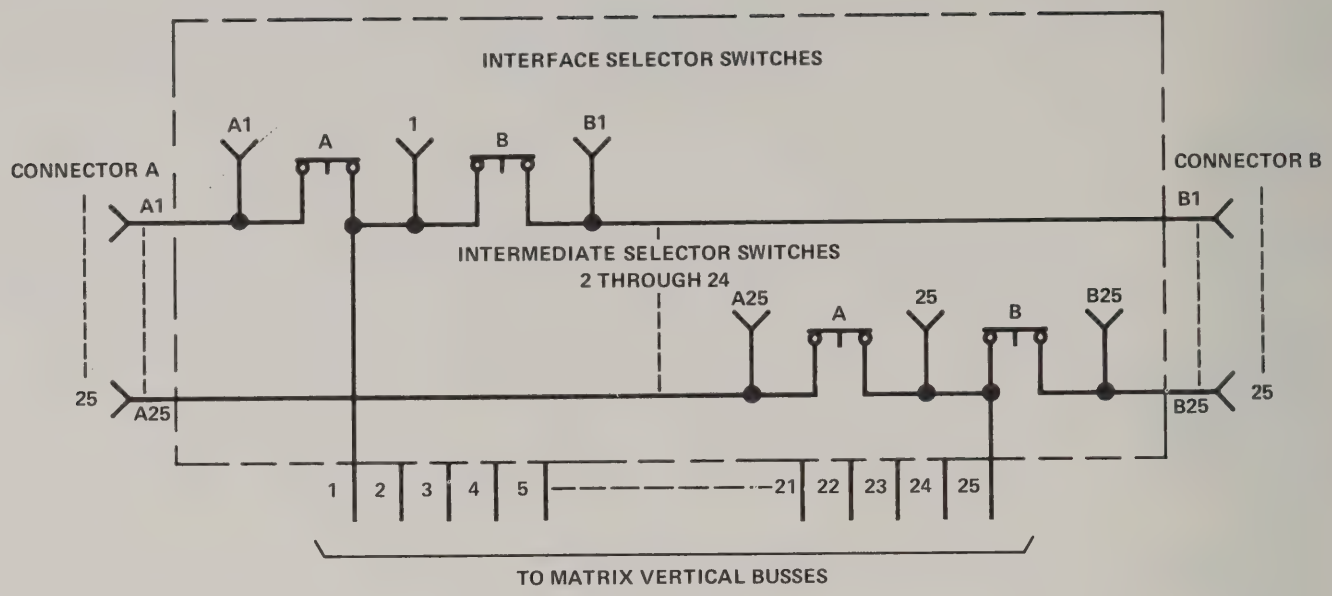


Figure 5-1. Interface Selector Switches, Schematic Diagram

To measure, for example, a positive pulse, set the TRIGGER TP1 switch to +/OPEN and the TRIGGER TP2 switch to -/CLOSE. The interval so measured is the pulse width.

5.08 **Meter**: The front-panel meter can be used for the following purposes:

(a) To measure dc voltages on the interface leads.

(b) To measure ac voltages, dc voltages, or resistance to ground of an external circuit.

NOTE: One side of the ohmmeter is grounded.

5.09 To measure dc voltages on the interface leads, place the FUNCTION switch in the VOLT INT position, turn the RANGE switch to the appropriate dc range, and turn the VERTICAL MONITOR switch to the desired interface lead number. The NOR position of the POLARITY switch gives an up-scale reading for positive inputs.

5.10 To measure ac voltage, dc voltage, or resistance to ground in an external circuit, connect the circuit to the INPUT terminals, turn the FUNCTION switch to VOLT/OHM EXT, and turn the RANGE switch to the appropriate voltage or resistance range. The ac meter input is a balanced high-impedance circuit to produce minimum loading when connected across a telephone line.

CAUTION: Damage may result to the meter when measuring line signals (FUNCTION switch set to EXT) if the RANGE switch is inadvertently placed in the DCV or X1, X100 (ohms) position. The FUNCTION switch should be set to OFF when the set is being transported.

5.11 **Loudspeaker**: To audibly monitor the signal on a line, connect the line to the INPUT terminals, turn the FUNCTION switch to SPKR, and adjust the volume with the RANGE switch in its ACV positions. The ability to listen to the line signals is, at times, helpful in identifying system problems. Noise, clicks, and crosstalk, for example, can frequently cause data transmission problems.

Testing Serial Data Sets

5.12 Connect the data set to the test set by means of the A or B connector. Insert pins in the program matrix for the proper interconnections between the data set and the test set. Set the INTERFACE MODE switch to VOLTAGE or CONTACT as required; this setting will usually be VOLTAGE for serial data sets. Set switches S1 through S8 to place control signals on the appropriate interface leads, and observe lamps DS1 through DS8 for the proper response.

5.13 The most common test is the end-to-end test which is depicted in Figure 5-2A. The overall performance of the total system, i.e., transmitting data set, telephone line, receiving data set, is checked in this test.

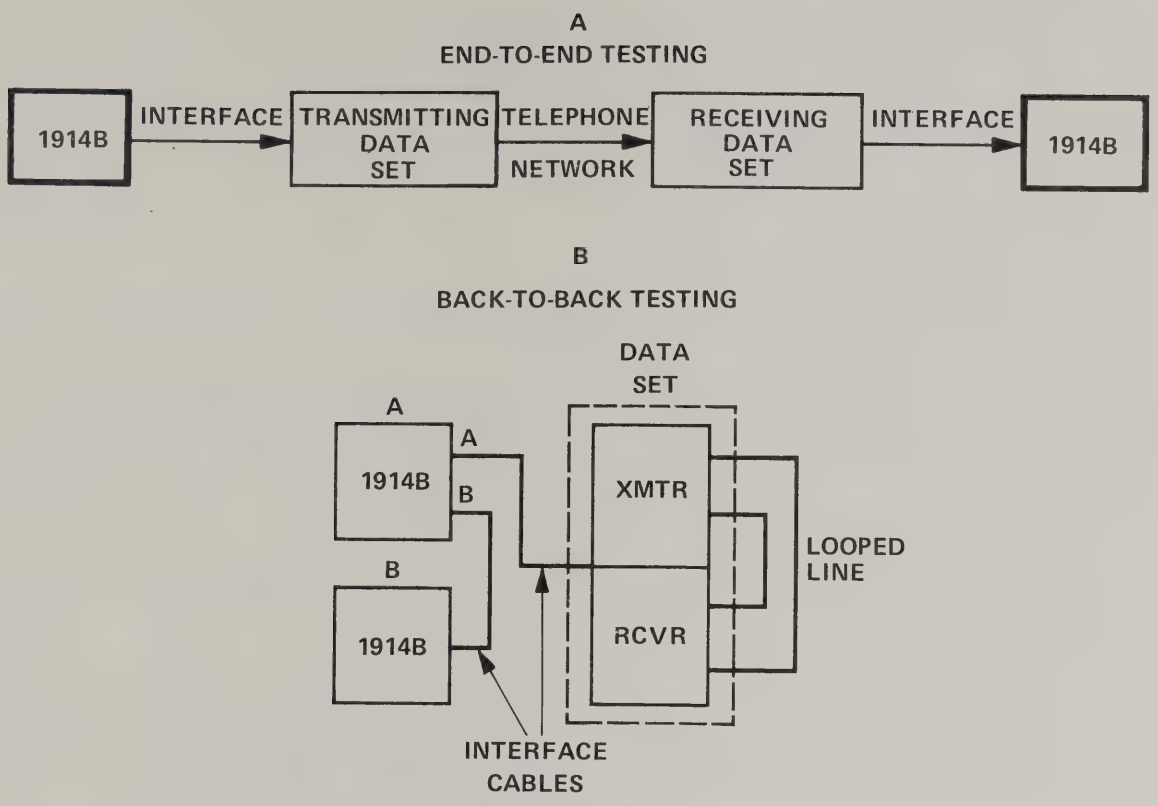


Figure 5-2. Typical Test Setups

The test set at the transmitter and receiver location are operated in the transmit and receive modes, respectively. Upon completion of the tests in the direction shown – if the system being tested is half-duplex or full duplex, the tests can be repeated in the opposite direction.

5.14 To test a full-duplex data set back-to-back, the line signal output from the transmitter must be looped back to the receiver line input. The test still requires two 1914B test sets, one operating as a controlling test set (A) and the second as a slave unit as shown in Figure 5-2B. Set A is connected to the data set by means of the interface cable which carries both the transmit as well as the receive signals. Set A should be programmed to operate all the control functions of the data set; test set B functions only as a data generator or comparator. The connections between sets A and B are most easily established by means of a second interface cable. Set B is programmed to connect to only the transmit (i.e., SD, SCT) or receive (i.e., RD, SCR) signal leads. The actual test is performed in the normal manner as described in 5.17 through 5.19.

5.15 The input/output leads of the test set are assigned to the horizontal buses of the matrix in such an order that the program for most data sets requires placing pins approximately along a diagonal line, as shown in Figure 5-3, which is intended as an illustration only. Pin 1 of the interface (EIA circuit AA; CCITT-circuit 101) is connected to the GRD bus as is pin 7 (circuit AB; 102). Pin 2 (BA; 103) connects to the SD bus which carries the word generator output. Similarly, pin 3 (BB; 104) is connected to the RD bus, which accepts the received data input when the test set is in the receive mode. The transmit and receive clock signals from the data set (circuits DB, DD; 113, 115), respectively, appear on the SCT and SCR buses. Switches S1, S5, S6, and S7 apply control signals to the "Send Request" lead (CA; 105), the "Data Terminal Ready" lead (CD; 108), the "Secondary Request to Send" lead (SCA; 120), and to the "Data Signal Rate Selector" lead (CH/CI; 111/112), respectively. S4 is used to simulate a low-speed "Secondary Transmitted Data" input (lead SBA; 118). Lamps DS1 through DS8 are programmed to monitor the output of the data set on, respectively, the "Clear to Send" lead (CB; 106), the "Data Set Ready" lead (CC; 107), the "Received Line Signal Detector" lead (CF; 109), the "Secondary Line Signal Detector" lead (SCF; 122), the "Secondary Clear to Send" lead (SCB; 121), the low-speed "Secondary Received Data" Signal lead (SBB; 119), the "Signal Quality Detector" lead (CG; 110), and the "Ring Indicator" lead (CE; 125).

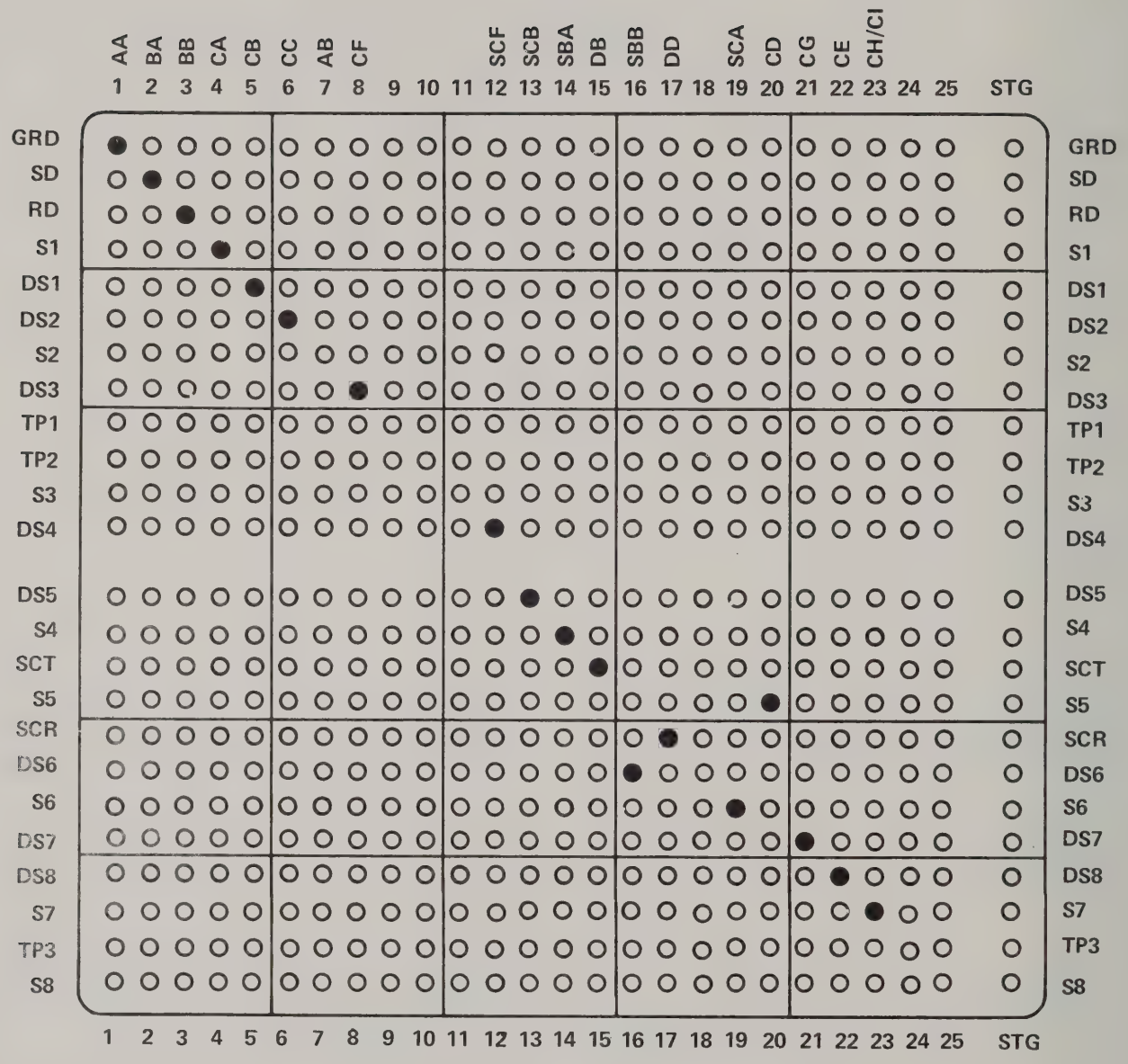


Figure 5-3. Sample Program of Matrix

5.16 **Indicator Lights:** If the NO DATA or NO CLOCK lamp lights during an error rate test, a malfunction is indicated. The malfunction must be present for several seconds to light these lamps.

5.17 **Transmitting Tests – Synchronous or Asynchronous Data Sets:**

Step 1
Set the TEST SET MODE switch to TRMT SET.

Step 2
For synchronous data sets, set the BIT RATE switch to EXT + or EXT –, depending on the desired phase relationship of clock signal to data signal; this setting will usually be EXT +.

For asynchronous data sets, set this switch to the appropriate bit rate.

Step 3
Set the SIGNAL LEVEL switch to the required position.

NOTE: For data sets conforming to EIA or CCITT specifications the signal level must be ±4 volts.

Step 4
Set the WORD LENGTH switch for the desired test signal.

5.18 **Receiving Tests – Synchronous Data Sets:**

Step 1
Set the TEST SET MODE switch to RCV SER.

Step 2
Set the WORD LENGTH switch to agree with the transmitted word.

Step 3
Set the COUNTER switch to BIT ERRORS or BLOCK ERRORS, as required. Block errors can only be counted with the WORD LENGTH switch set to 63 or 511.

Step 4
Set the BIT RATE to EXT + or EXT - depending on the desired phase relationship of clock signal to data signal (normally EXT +).

Step 5
Operate the WORD SYNC switch momentarily to MAN or set the switch to AUTO.

Step 6
Press the RESET switch momentarily to clear the counter.

Step 7
Observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

5.19 **Receiving Tests – Asynchronous Data Sets:**

Step 1
Set the TEST SET MODE switch to RCV SER.

Step 2
Set the WORD LENGTH switch to agree with the transmitted word.

Step 3
Set the COUNTER switch to BIT ERRORS or BLOCK ERRORS as required. Block errors can only be counted when the WORD LENGTH switch is set to 63 or 511.

Step 4
Set the PHASE control to mid position, with the dot pointing up.

Step 5
Set the BIT RATE switch to agree with the transmitted bit rate.

Step 6
Set the FUNCTION switch to PHASE ADJ.

Step 7
Adjust the PHASE control for a null on the meter.

Step 8
Set the FUNCTION switch to some position other than PHASE ADJ (do not return to PHASE ADJ during remainder of test).

Step 9
Set the SAMPLE WIDTH switch to .5 μs.

Step 10
Operate the WORD SYNC switch momemtarily to MAN, or set it to AUTO.

Step 11
Set the SAMPLE WIDTH switch to the desired sampling interval for error margin testing.

Step 12
Press the RESET switch momentarily and observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

Step 4
Set the TEST SET MODE switch to RCV 402.

Step 5
Set the COUNTER switch to BIT ERRORS or BLOCK ERRORS as required.

Step 6
Set the TEST MODE switch to ALL RDM to test all eight channels simultaneously; set the switch to CHAN/1-8 to check any channel individually.

Step 7
Operate the WORD SYNC switch momentarily to MAN or set it to AUTO.

Step 8
Press the RESET switch momentarily to clear the counter.

Step 9
Observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

Testing Analog Data Sets

5.24 Analog data sets can be tested by applying precision dc voltages to the transmitter (SD lead) and measuring the receiver (RD) output voltage. The interface connections are established on the program matrix and the data set control functions are checked by using S1 through S8 and DS1 through DS8, as discussed in 5.12 – 5.15.

5.25 **Transmitting Tests:**

Step 1
Set the REFERENCE VOLTAGE SELECT switch to the desired fixed voltage or to the ADJ position.

Step 2
Set the OUTPUT switch to TP3.

Step 3
Insert a shorting pin at the intersection of the TP3 horizontal bus and the vertical bus connected to the SD lead.

Step 4
Set the VERTICAL MONITOR switch to the position corresponding to the SD interface lead.

Step 5
If the adjustable voltage is to be used, turn the FUNCTION switch to VOLT INT, and the RANGE switch to the appropriate DCV range. Using the meter, set the voltage to the desired value.

Testing Parallel Data Sets

5.20 The tests described in the following paragraphs were designed for the WECO 402 type of modems.

5.21 Connect the data set to the C (transmit) or D (receive) connector. Insert pins in the program matrix for the proper interconnections of the interface control leads between the data set and the test set. (Refer to Figure 3-3.) Set the INTERFACE MODE switch to the CONTACT position. Set switches S1 through S8 to place control signals on the appropriate interface leads and observe lamps DS1 through DS8 for the proper response. Set the TEST MODE switch to ALL SPC to place a spacing condition on all channels, to ALL DOT to apply alternate marks and spaces to all channels, or to one of the eight channels to place a test word on that channel while applying a dot signal to all other channels.

NOTE: If the NO DATA or NO CLOCK lamp lights during an error rate test, a malfunction is indicated.

5.22 **Transmitting Tests:**

Step 1
Set the WORD LENGTH switch to select the desired test signal.

Step 2
Set the SIGNAL LEVEL switch to ±4 volts.

Step 3
Set the BIT RATE switch to EXT ±.

Step 4
Set the TEST SET MODE switch to TRMT 402.

Step 5
Set the TEST MODE switch to ALL RDM to test all eight channels simultaneously or any one channel individually.

Step 6
Set the TRMT CLOCK PHASE switch to RET, NOR, or ADV, as required. In an end-to-end test this control at the

transmitting data test set may be set to the ADV or RET position which will change the phase relationship between the clock signal and the data signal by 1.5 ms. This establishes a marginal condition which will normally result in increased errors at the receiving data set.

5.23 **Receiving Tests:**

Step 1
Set the WORD LENGTH switch to select the desired test signal.

Step 2
Set the SIGNAL LEVEL switch to ±4 volts.

Step 3
Set the BIT RATE switch to EXT ±.

5.26 **Receiving Tests:**

Step 1
Set the VERTICAL MONITOR switch to the position corresponding to the RD interface lead.

Step 2
The measured voltage should be the same, both in magnitude and polarity, as the transmitted voltage within the modem manufacture's specified circuits.

5.27 **4-dB Pad.** The 4-dB pad may be shunted across the output line of the transmitting data set during error rate tests. The resultant bridging loss reduces the signal level by about 4 dB and, therefore, also reduces the signal-to-noise ratio at the receiving data set. Consequently, the test conditions are more stringent than those encountered during normal operation of the data set.

SECTION 6
CIRCUIT DESCRIPTION

GENERAL

6.01 This section provides a discussion on logic gates and flip flops followed by a detailed discription of the circuits comprising the 1914B test set. Most of the test set circuitry is comprised of circuit packs (CP's) or circuit boards with designations from CP1 through CP5 and CP8 through CP14. These CP's individually and severally form the major circuits of the test set. The functional schematics for these major circuits are listed in the table below and are discussed in detail in this section with the exception of the lamp driver and accessory schematic, Figure 6-28. Following the functional schematics are the individual circuit schematics for the CP's which offer more circuit detail than the functional schematics. Following the CP schematics are details on the integrated circuits used in the test set.

Table 6-1. Functional Schematics

Figure	
6-19	Interface Connections
6-20	Clock Circuit
6-21	Word Generator and Word Sync Recovery Circuit
6-22	Error and Interval Counter Circuit
6-23	Parallel Data Transmit Circuit
6-24	Parallel Data Receive Circuit
6-25	Reference Voltage Circuit
6-26	Meter Circuit
6-27	Power Supply
6-28	Lamp Drivers, Program Pins, Interface Cables, and 4 dB Pad

Logic Gates and Flip-Flops

6.02 Logic OR, exclusive-OR, NOR (not-OR), AND, inhibited-AND, and NAND (not-AND) gates are used in the test set along with flip-flop (FF) multivibrators, level converters (logic interface), a decade counter BCD out), and a decimal decoder/driver (BCD-to-Nixie). The following description of logical functions is applicable to both discrete and integrated circuits, although only one or the other may be used.

6.03 As shown by Figure 6-1, the positive-AND gate provides a high output only when all inputs are high. The gate "conducts" whenever any of its inputs is relatively negative (i.e., low or 0), causing a low output. The circuit is also properly termed a negative-OR gate.

TRUTH TABLE

A	B	X
1	1	0
1	0	1
0	1	1
0	0	1

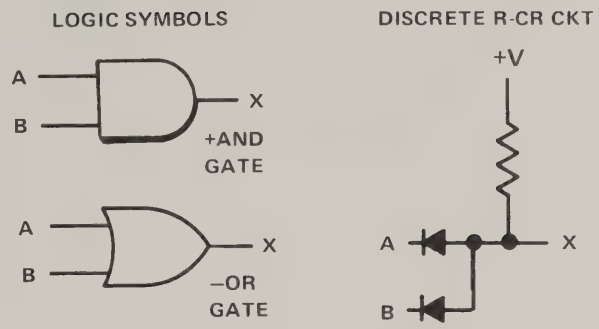


Figure 6-1. Basic AND/OR-Gate Logic

6.04 As shown by Figure 6-2, both the NAND gate (a not-AND or inverting-AND gate) and the NOR gate (a not-OR or inverting-OR gate) produce a relatively negative (i.e., low or 0) output while both inputs are high. Conversely, any low input holds the output at its high level. The NAND gate can be considered to be a coincidence circuit that produces a high or 1 output except when all inputs are concurrently high or 1, during which time it produces a low or 0 output. With NAND-gate logic, the occurrence of coincident-1 inputs and the resulting 0-output level is often of principal importance. The NOR gate can likewise be considered to be a coincidence circuit; however, NOR-gate logic tends to emphasize the occurrence of 0-level inputs and the resulting 1-output level. The logical functioning of the NAND and NOR gates is the same, but different symbols are used so as to better represent the particular application.

6.05 With two or more inputs, either the NAND or the NOR gate serves as a logical-decision point, although such gates can also function as simple inverters when only a single input is used. Because gate-output level is contingent upon gate-input levels, an input may be held at or changed to a particular level so as to either enable or inhibit the gate as appropriate. For instance, a NAND gate

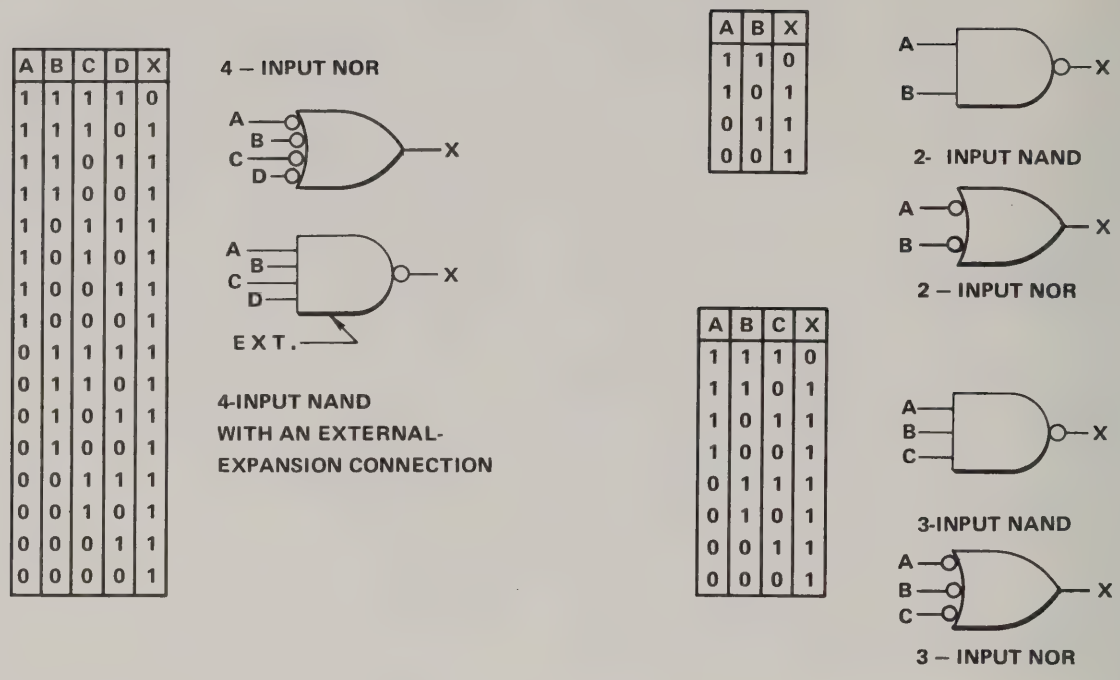


Figure 6-2. NAND/NOR-Gate Logic

is inhibited by any input that remains at 0 while all other inputs are at I, being enabled only when that input goes from 0 to 1; after being so enabled, a 0 output results when the other inputs next go to 1.

6.06 As shown by Figure 6-3, the NAND gate is also used with only one input (as can be the NOR gate), having unused-input lead(s) unconnected – equivalent to the high or 1 level – or having all inputs connected in parallel. With either arrangement, the gate functions as an inverter, or inverting amplifier. (A low input produces a high output; conversely, a high input produces a low output.) A logic-level inversion is thus provided.

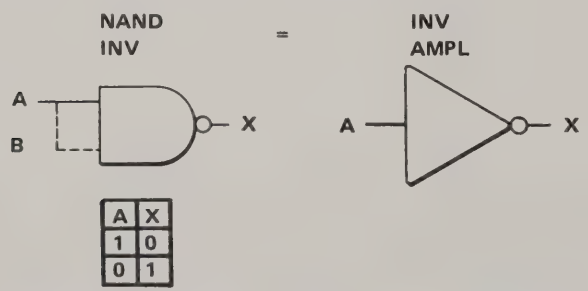


Figure 6-3. NAND-Gate Inverter (Inverter Amplifier).

6.07 As shown by Figure 6-4, the two-input exclusive-OR gate provides a high output when either input is high, but the gate "conducts" whenever both inputs are either high or low, causing a low output. This is a unique "either-OR, but not both" circuit that is also properly termed an AND-NOR gate.

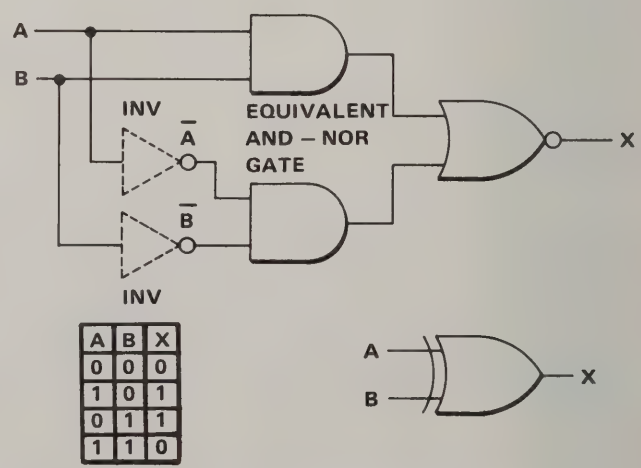
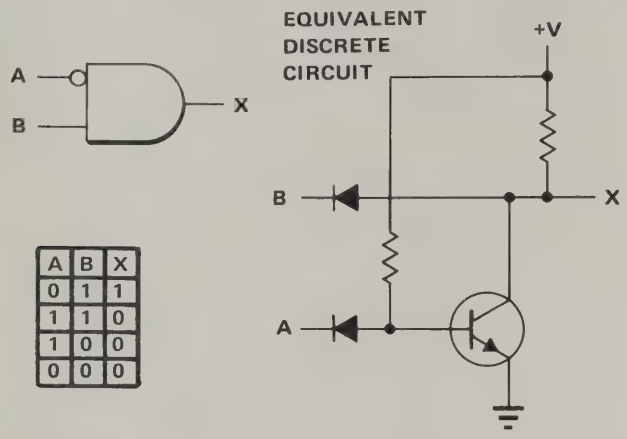


Figure 6-4. Exclusive-OR Gate Logic.

6.08 As shown by Figure 6-5, the two-input inhibited-AND gate has a suppressor, or inhibitory, input and a regular input, providing an uninverted output that corresponds to its normal-input level (either high or low) unless the output level is clamped by an inhibiting input. (Note that a 1/high-B input appears at the output only when there is a 0/low-A input; thus, a controlled delay is obtained when the 0/low-suppressor input occurs after the 1/high-regular input is applied.)



A	B	X
0	1	1
1	1	0
1	0	0
0	0	0

Figure 6-5. Inhibited- AND Gate Logic

6.09 As shown by Figure 6-6, the basic R-S/latch FF is derived from two symmetrically cross-connected inverting-NAND gates. For bistable operation, the R-S FF will "latch" in either of its two stable states, changing from one to the other only when triggered by an appropriate reset (R) or set (S) input. This allows it to be used as a storage element because – once triggered into one or the other state – it remains "toggled" whether or not the initial-triggering level is maintained. By using additional inputs to the NAND gates, several set and/or reset inputs may jointly control the FF-output states. Although operation of the basic R-S FF is asynchronous (i.e., no clock-pulse input is required), the FF can be external-clock synchronized by adding a two-input NAND gate being tied to a common clock-pulse source. (A third stable state, allowing seldom-used tristable operation, is obtained when low/0 signals are simultaneously applied to the R and S inputs, causing both outputs to go to the high/1 state.)

IN		OUT	
S	R	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	‡	‡
0	0	1	1

‡NO CHANGE

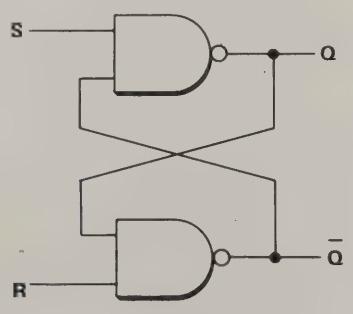


Figure 6-6. Basic R-S/Latch Flip-Flop

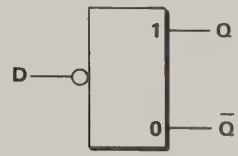
6.10 As shown by Figure 6-7, the O-S (one-shot) FF is a monostable multivibrator with one stable state and one quasistable state. When triggered, the FF temporarily changes state, returning to its original, stable state after an interval that is determined by its R-C time constant. (For an IC-OS FF such as IC4/9941, the requisite time constant is provided by an external-capacitor and internal-resistor combination.) This circuit is also termed a delay (D-type) FF.

6.11 Also shown by Figure 6-7 is a clocked O-S FF for synchronous operation. In this version, the logic level at the S (or D) input appears at the Q output following the C-input transition.

A. OS–DELAY FF

	t_D		t_{R-C}	
D	Q	$\overline{Q}$	Q	$\overline{Q}$
0	0	1	1	0
1	1	0	0	1

t_D = D-INPUT TRANSITION
t_{R-C} = DELAY-TIME END



B. CLOCKED OS-DELAY FF

	t_n		t_{n+1}	
D	Q	$\overline{Q}$	Q	$\overline{Q}$
0	1	0	0	1
1	0	1	1	0

t_n = TIME INTERVAL BEFORE CLOCK-IN TRANSITION
t_{n+1} = TIME INTERVAL AFTER CLOCK-IN TRANSITION

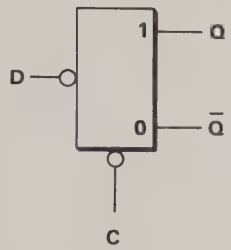


Figure 6-7. O-S (Delay) Flip-Flop

6.12 As shown by Figure 6-8, the T-type FF has a trigger (T) input and a clock (C) input as well as two outputs (Q and $\overline{Q}$). With a high/1-T input, the FF synchronously toggles between its two operating states in response to the clock input. However, the FF cannot toggle with a low/0-T input, which inhibits operation.

T	C	Q	$\overline{Q}$
1	0	T	T
1	1	T	T
0	0	‡	‡
0	1	‡	‡

‡ = NO CHANGE
T = TOGGLES

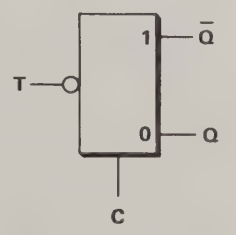


Figure 6-8. Synchronous-T Flip-Flop

6.13 As shown by Figures 6-9 through 6-12, the R-S/J-K and J-K types of FF are similar, with both having the usual outputs (Q and $\overline{Q}$), two "synchronous" inputs (J and K or the equivalent), and a clock/trigger (T) input. The R-S/J-K FF (i.e., IC5/9945), has "asynchronous" direct-set (S_D) and direct-clear (C_D) inputs as well; however, the J-K FF (i.e., IC6/9094 and IC7/9097) has only the S_D input. As implied by its designation, the R-S/J-K FF can be used as either an R-S or a J-K FF, normally operating in the R-S mode but readily convertible to J-K type FF is determined by several unique characteristics as well as by certain external-circuit connections. Like any bistable FF or multivibrator (including the R-S FF), it has two stable states, changing from one to the other in response to an external signal providing that it is conditioned to do so. The Q and Q outputs of the J-K FF can respectively be either 1 and 0 or 0 and 1, as controlled by the J and K inputs and by the T, S_D, and (if used) C_D inputs. However, when the "clocked" R-S mode of the convertible R-S/J-K FF is used, an indeterminate-output condition can result when the J and K (S... and C...) inputs are simultaneously set to the same level and the FF is triggered. This ambuiguity cannot occur in J-K operation.

6.14 In the asynchronous R-S mode, operation of the R-S/J-K FF is controlled by the direct-set (S_D) and direct-clear (C_D) inputs as shown by Figure 6-9. (The other, synchronous S..., C..., and T inputs are unused in the asynchronous mode.)

SET (S_D)	CLEAR (C_D)	t_{n+1} Q	t_{n+1} $\overline{Q}$
0	0	1	1
1	0	0	1
0	1	1	0
1	1	‡	‡

‡ NO CHANGE WITH SYNCHRONOUS INPUTS UNUSED

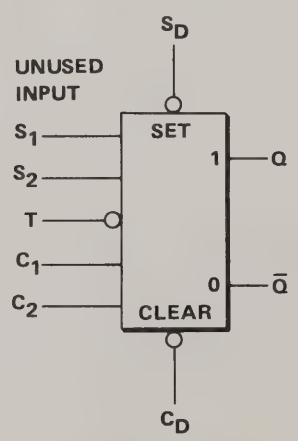


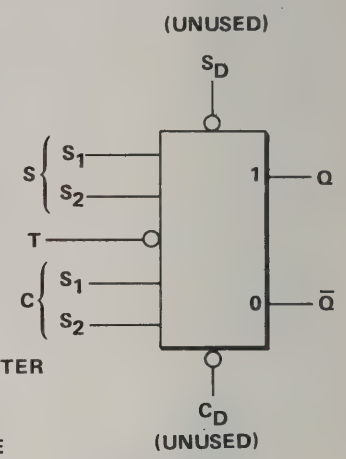
Figure 6-9. R-S/J-K Flip-Flop (R-S Mode of IC5/9945)

6.15 In the synchronous (clocked) R-S mode (Figure 6-10), the output of the R-S/J-K FF is a function of the S... and C... inputs at the time of a negative-going clock/trigger (T-input) transition. A change in the S... and/or C... input(s) is only effective when the clock/trigger-T input is at the high/1 level, with any resulting change in the FF-output state occurring on the trailing edge (0-to-1 transition) of the T-input signal. When the S_1 and S_2 and the C_1 and C_2 inputs are separately connected, the FF will toggle or change state only when triggered while both of the S inputs or both of the C inputs, as appropriate, are simultaneously at the high/1 level.

EXPANDED TRUTH TABLE

S_1	S_2	C_1	C_2	t_{n+1} Q	t_{n+1} $\overline{Q}$
0	–	0	–	‡	‡
0	–	–	0	‡	‡
–	0	0	–	‡	‡
–	0	–	0	‡	‡
0	–	1	1	0	1
–	0	1	1	0	1
1	1	0	–	1	0
1	1	–	0	1	0
1	1	1	1	?	?

t_{n+1} = TIME INTERVAL AFTER CLOCK/TRIGGER
‡ = NO CHANGE FROM LEVELS AT t_n (TIME INTERVAL BEFORE CLOCK/TRIGGER)
? = INDETERMINATE



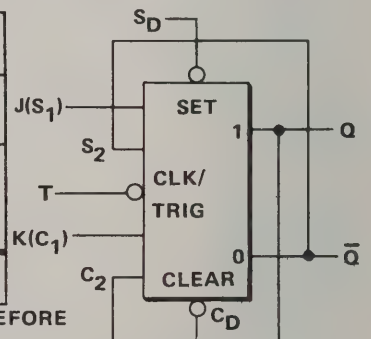
SIMPLIFIED TRUTH TABLE

S (S_1 & S_2)	C (C_1 & C_2)	t_{n+1} Q	t_{n+1} $\overline{Q}$
0	0	†	†
0	1	0	1
1	0	1	0
1	1	?	?

Figure 6-10. R-S/J-K Flip-Flop (Clocked R-S Mode of IC5/9945)

6.16 For the J-K mode of operation of the R-S/J-K FF (Figure 6-11), its Q and S_2 leads are cross-coupled by means of an external connection as are its Q and C_2 leads. The S_1 and C_1 leads are respectively used as the J and K inputs. Either one or both of the direct-set (S_D) and direct-clear (C_D) inputs may be used to "preset" and/or condition the FF. When properly conditioned and with appropriate J and K inputs, the FF toggles or changes state on the trailing edge (1-to-0 transition) of the clock/trigger (T) input signal. (Some special characteristics of the J-K type FF are outlined in the following paragraph, 6.19.)

SET (S_D)	CLEAR (C_D)	t_n J (S_1)	t_n K (C_1)	t_{n+1} Q	t_{n+1} $\overline{Q}$
1	1	1	1	*	*
1	1	1	0	1	0
1	1	0	1	0	1
1	1	0	0	‡	‡
1	0	–	–	0	1
0	1	–	–	1	0



t_n = TIME INTERVAL BEFORE CLOCK/TRIGGER
t_{n+1} = TIME INTERVAL AFTER CLOCK/TRIGGER
* = CONVERSE OF LEVELS AT t_n
‡ = NO CHANGE FROM LEVELS AT t_n

Figure 6-11. R-S/J-K Flip-Flop (J-K Mode of IC5/9945).

6.17 As shown by Figure 6-12, the J-K FF has two inputs (J and K) and two outputs (Q and $\overline{Q}$) along with clock/trigger (T) and direct-set (S_D) inputs, which are respectively used to trigger and to "preset" and/or condition the FF. Operation of the J-K type FF is determined by several unique characteristics as well as by certain external-circuit connections. Like any bistable FF or multivibrator, it has two stable states, changing from one to the other in response to an external signal providing that it is properly conditioned to do so. The Q and Q outputs can respectively be either 1 and 0 or 0 and 1, as controlled by the J and K inputs and by the T and/or S_D inputs (also by the C_D input in the instance of the convertible R-S/J-K FF that is used in the J-K mode). Some characteristics of the J-K type FF are outlined below.

(a) The FF "complements" or toggles only under well-defined conditions.

(b) With the S_D-input level and both the J and K inputs at 1/high, the FF changes state or toggles on the trailing edge (1-to-0 transition) of the next clock/trigger (T) input signal. There is an inherent delay between the time of triggering and the time at which toggling occurs. (If the J and K inputs are held at the 1/high level, the FF toggles once every clock/trigger-input cycle, thus operating as a divide-by-two counter.)

(c) With the J and K inputs at opposite levels (e.e., J at 1/high and K at 0/low, or vice versa), the Q output goes to the same level as that of the J input on the trailing edge of the next clock/trigger signal.

(d) Both the J and K inputs ordinarily remain constant while a clock/trigger signal (defined as a 0/low level at the T input) is applied.

(e) With both J and K inputs at 0/low, the FF does NOT toggle during the clock/trigger-input signal, but remains in its prior condition.

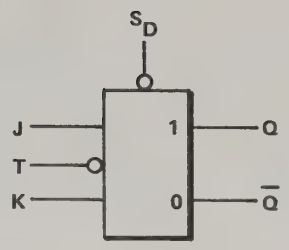
(f) Changes in the J-and-K inputs are effective only when the clock/trigger-input signal is at 1/high (S_D and, if used, C_D must also be at 1/high).

(g) With S_D at 1/high, the FF can toggle as just noted. When S_D goes to 0/low (regardless of other input levels), output Q is set to 1/high (and $\overline{Q}$ is conversely set to 0/low).

(h) In the instance where an additional C_D input is provided, the FF can toggle as previously noted while both S_D and C_D are at 1/high. When C_D goes to 0/low (regardless of other input levels), output Q is set to 0/low (and Q is conversely set to 1/high).

NOTE: Direct-set (S_D) and, if used, direct-clear (C_D) override the synchronous J, K, and T inputs. The "direct" inputs are completely independent of the other inputs.

SET (SD)	t_n		t_{n+1}	
	J	K	Q	$\overline{Q}$
1	1	1	*	*
1	1	0	1	0
1	0	1	0	1
1	0	0	‡	‡
0	–	–	1	0



t_n = TIME INTERVAL BEFORE CLOCK/TRIGGER

t_{n+1} = TIME INTERVAL AFTER CLOCK/TRIGGER

* = CONVERSE OF LEVELS AT t_n

‡ = NO CHANGE FROM LEVELS AT t_n

Figure 6-12. J-K Flip-Flop (IC6/9094 and IC7/9097)

1914B Circuit Description

6.18 **Interface Connections (Figure 6-19).** Various connections at the interface between data-communications and data-terminal equipment (DCE and DTE, respectively) are possible by means of a multipoint-program matrix and 25 interface-selector switches. The INTERFACE MODE selector switch, S18, allows operation in either the contact or the voltage interface-signal modes. (See also Section 3, Functional Description.)

6.19 Interconnection with the equipment under test may be made via front-panel connectors J1 (A) and/or J2 (B). Alternatively, interconnection with Western Electric 402-type or with other parallel-channel equipment may be made via connectors J3 (C) and/or J4 (D). All four of these are standard 25-pin connectors that mate with most DTE-DCE cables and with the interface-connection cables of the test set. Any or all of the individual pins of connectors J1 and/or J2 can be connected to the internal circuits of the test set via the bank of interface-selector switches and the program matrix. Ten pins of connectors J3 and J4 are cross-connected (e.g., J3-13 to J4-13) and are also wired directly to the program matrix, as is J3-17. Other pins of J3 connect directly to circuit ground or to the parallel data transmit circuits (see FS5). Any or all of these 11 pins that are wired to the program matrix can be connected to the internal circuits of the test set as required, bypassing the interface-selector switches. Other pins of J4 connect directly to circuit ground or to the parallel data receive circuits (see FS6).

6.20 Each of the 25 push-pull interface-selector switches has two series-connected sections identified as A and B. One contact of the A section connects with one pin of J1 and one contact of the B section connects with a corresponding pin of J2. The other contact of the A section has a common connection with the other contact of

the B section which in turn has a common connection to one of the 25 vertical buses. These vertical buses are individually terminated by high-value (300 kilohm) resistances, R1 through R25. By opening and/or closing switch-sections 1A and 1B through 25A and 25B, the desired bridging and/or terminating connections can be made with the equipment under test. EIARS-232/CCITT-V.24 interface-connection assignments are listed in Table 6-2. Corresponding signal-interchange circuits are listed by category in Table 6-3.

6.21 The crosspoint-type program matrix has 25 vertical and 24 horizontal buses that are connected as necessary by manually inserting "program pins" (e.g., shorting pins) at the appropriate vertical-to-horizontal intersections. There are three types of program pins. When series resistance is required, either a program pin with a built-in 10-ohm resistance or one with a built-in 18-ohm resistance can be used in lieu of the direct-shorting pin. Although the data, timing (if used) and control signals that appear on the vertical buses are contingent upon the specific pin assignments for the interface connector of the equipment under test, the horizontal buses are dedicated to certain functions being connected to specific switches, indicators, and other circuits of the test set.

6.22 Eight of the horizontal buses individually connect with respective channel ON-OFF switches, S1-S8, via multisegment INTERFACE MODE switch S18. Another eight horizontal buses individually connect with respective CONTROL SIGNAL indicators, DS1-DS8, via the INTERFACE MODE switch and (if the VOLTAGE mode is selected) the lamp-driver circuits (see Figure 6-25). Of the remaining eight horizontal buses, one connects directly to circuit ground and the other seven connect to test-set circuits as listed below.

(a) SD (send data or transmitted data) connects with the output amplifier of the word generator and sync recovery circuit via TEST SET MODE switch S20 when the TRMT SER mode is selected (see Figure 6-21).

(b) RD (receive data) connects with the data-shaping and data (phase) comparator section of the clock circuit via TEST SET MODE switch S20 when the RCV SER mode is selected (see Figures 6-24 and 6-20).

(c) TP1 and TP2 connect with respective input amplifiers of the error and interval counter circuit via COUNTER switch S21 when the X.1, X1, X10, or X100 mS mode is selected (see Figure 6-22).

(d) SCT (serial clock transmit) or SCR (serial clock receive) connect with the input to the clock shaping-and-logic circuits of the clock circuit via TEST SET MODE switch S20. With S20 turned to TRMT SER, SCT is connected. With S20 turned to RCV SER, SCR is connected. (See Figures 6-23 and 6-20.)

(e) TP3 connects with the reference voltage circuit via OUTPUT switch S10 and SELECT switch S9 when S10 is placed in TP3, with the dc-reference voltage on TP3 being controlled by S9. (See Figure 6-24.)

6.23 Any 1 of the 25 vertical buses in the program matrix can be selected by VERTICAL MONITOR switch S19 for monitoring by the front-panel meter. The IM (internal monitor) lead from S19 connects with the meter circuit via FUNCTION switch S22 when turned to VOLT INT, with the meter range and polarity being respectively controlled by S23 and POLARITY switch S26. (See Figure 6-26.)

6.24 **Clock Circuit (Figure 6-20).** The clock circuit, used in both transmit and receive modes, generates the timing signals for driving the word generator and comparator. The rate of timing signals generated depends on the setting of the BIT RATE switch.

6.25 When the TEST SET MODE switch is in the TRMT-SERIAL position, a contact of that switch is grounded and connected to pin Y of a lowpass filter on CP1. This causes the voltage control oscillator on CP1 to generate a positive going sawtooth wave. The rate of generation is dependent on the position of the BIT RATE switch which controls the connection of the CP10 capacitors to the oscillator circuit. The generated sawtooths are applied to the three slicers through an isolation buffer amplifier. Slicer 1-"one" transforms the sawtooth to a symmetrical square wave which appears at the outputs of IC1-1B and IC2-1C. The output of IC2-1C is used as a clocking signal in the word generator circuit (Figure 6-21).

6.26 The output of IC2-1C is also applied to the IC5-1 phase comparator. In the receive mode of operation another input to this phase comparator is applied from the transition detector which detects transitions in the signal level applied to pin 27 and provides an output pulse to the comparator for each transition. The incoming signal, before being applied to the detector, is limited to prevent overvoltages and to establish a reference level. The signal is then conditioned by a lowpass filter and feedback slicer circuit to reduce noise susceptibility and provide a logic level signal.

6.27 The two inputs to the phase comparator are combined to produce a square wave output with an equivalent dc level of 2.4 volts when the two inputs are in phase and an equivalent dc level which varies above or

Table 6-2. Pin Assignments for Data-Interface Connector per EIA Recommended Standard 232 (Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange).

PIN NO.	EIA ASSIGNMENT* (RS-232B/RS-232C)	EIA RS-232 CIRCUIT	CCITT V.24 CIRCUIT
1	Protective Ground	AA	101
2	Transmitted Data	BA	103
3	Received Data	BB	104
4	Request to Send	CA	105
5	Clear to Send	CB	106
6	Data Set Ready	CC	107
7	Signal Ground/Common Return	AB	102
8	Data Carrier Detector (Received Line Signal Detector)*	CF	109
9	Reserved for Data Set Testing	–	–
10	Reserved for Data Set Testing	–	–
11	Unassigned	–	–
12	Unassigned (Secondary Received Line Signal Detector)*	(SCF)*	122
13	Unassigned (Secondary Clear to Send)*	(SCB)*	121
14	Unassigned (Secondary Transmitted Data)*	(SBA)*	118
15	Transmission Signal Element Timing – DCE Source	DB	114
16	Unassigned (Secondary Received Data)*	(SBB)*	119
17	Receive Signal Element Timing – DCE Source	DD	115
18	Unassigned	–	–
19	Unassigned (Secondary Request to Send)*	(SCA)*	120
20	Data Terminal Ready	CD	108
21	Unassigned (Signal Quality Detector)*	(CG)*	110
22	Ring Indicator	CE	125
23	Unassigned (Data Signal Rate Selector – DTE/DCE Source)*	(CH/CI)*	111/112
24	Transmit Signal Element Timing – DTE Source	DA	113
25	Unassigned	–	–

*Where RS-232C assignment differs from that of RS-232B, the RS-232C information is given in parenthesis.

Table 6-3. EIA Signal-Interchange Circuits by Category.

Interchange Circuit	CCITT Equivalent	Description	Gnd	Data		Control		Timing	
				From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
AA	101	Protective Ground	X						
AB	102	Signal Ground/Common Return	X						
BA	103	Transmitted Data			X				
BB	104	Received Data		X					
CA	105	Request to Send					X		
CB	106	Clear to Send				X			
CC	107	Data Set Ready				X			
CD	108.2	Data Terminal Ready					X		
CE	125	Ring Indicator				X			
CF	109	Received Line Signal Detector				X			
CG	110	Signal Quality Detector				X			
CH	111	Data Signal Rate Selector (DTE)					X		
CI	112	Data Signal Rate Selector (DCE)				X			
DA	113	Transmitter Signal Element Timing (DTE)							X
DB	114	Transmitter Signal Element Timing (DCE)						X	
DD	115	Receiver Signal Element Timing (DCE)						X	
SBA	118	Secondary Transmitted Data			X				
SBB	119	Secondary Received Data		X					
SCA	120	Secondary Request to Send					X		
SCB	121	Secondary Clear to Send				X			
SCF	122	Secondary Rec'd Line Signal Detector				X			

Table 6-4. Pin Allocations for 1914B-Interface Connectors J3/C and J4/D (Signal Interchange with Parallel-Channel Data Equipment)

PIN NO.	TRANSMIT CONNECTOR J3/C	RECEIVE CONNECTOR J4/D
1	Ground	Ground
2	Transmit Channel 1	Receive Channel 1
3	Transmit Channel 2	Receive Channel 2
4	Transmit Channel 3	Receive Channel 3
5	Transmit Channel 4	Receive Channel 4
6	Timing Channel (Transmit)	Timing Channel (Receive)
7	Transmit Channel 5	Receive Channel 5
8	Transmit Channel 6	Receive Channel 6
9	Transmit Channel 7	Receive Channel 7

Table 6-4 (Cont)

PIN NO.	TRANSMIT CONNECTOR J3/C	RECEIVE CONNECTOR J4/D
10	Transmit Channel 8	Receive Channel 8
11	Ground	Ground
12	–	Ground
13	*	*
14	*	*
15	*	*
16	*	*
17	*	Ground
18	*	*
19	*	*
20	*	*
21	*	*
22	*	*
23	*	*
24	Ground	–
25	–	–

*Connects with corresponding vertical bus of program matrix in text set (i.e., both J3-20 and J4-20 connect with vertical-bus 20). For specific information concerning interconnection with Western Electric 402-type or other parallel-channel equipment, refer to the manufacturer's specifications and/or instructions for that equipment.

below the 2.4 volt level when there is a phase difference. The output of the comparator is applied to a lowpass filter on CP1 which substantially removes the components of the square wave and permits only the dc level to be applied to buffer amplifier IC10-1. The buffer amplifier is a difference amplifier which amplifies the difference between a 2.4 volt preset level within the amplifier and the dc level from the voltage comparator. The output of the amplifier will be 0 vdc when the two original inputs are in phase and at a positive or negative level for a phase difference, the sign being dependent on the phasing.

6.28 In a receive mode setting of the TEST SET MODE switch the output of the buffer amplifier is removed from ground and its output is the amplified difference described above. This difference voltage, which has any ripple component attenuated by a lowpass filter, is the error voltage applied to the voltage controlled oscillator to reduce any phase difference between the output of the oscillator and the received data signal.

6.29 The difference voltage from the buffer amplifier is also applied through a limiter to the meter M1 movement (see Figure 6-26) when the FUNCTION switch is set to PHASE ADJ. The deflection of the meter pointer observed at the start of a test is nulled by adjustment of the fine adjustment PHASE control R26 connected to the voltage controlled oscillator, and synchronization between the output of the oscillator and received data signal is nominally established. The phase control provides a means of varying the nominal oscillator frequency as much as ±10 percent to accomplish synchronization. The limiter prevents over voltages from damaging the meter movement.

6.30 Distortion generated on the incoming telephone line causes the transitions of the received signal to be affected by jitter so the lowpass filters described in the preceding paragraphs are employed to attenuate this jitter and prevent it from affecting the frequency of the voltage controlled oscillator. However, to effect initial synchronization quickly and over a wide frequency range, a reduction in the effect of the lowpass filters needs to be accomplished. Accordingly, capacitor C8 on CP12 (figure 6-20) is removed from pin 19 of CP1 when the FUNCTION switch is in the PHASE ADJ position. During the phase adjust period the disconnected capacitor is kept charged through a

reference voltage so that circuit disturbances will not result when the FUNCTION switch is set to a position other than PHASE ADJ. After initial adjustment the switch should be kept off this latter position.

6.31 The symmetrical square waves generated at the output of IC2-1C by the clock circuit is applied to the set input of single shot IC4-1. With the SAMPLE WIDTH set to .5 μs, the single shot delivers a negative going 0.5 μsec pulse to an output of gate IC1-2D during negative transitions of the clock signal. The other input to IC1-2D is held at a logical 1 since the input of IC2-2A through pin 5 is at a logical 0 when the SAMPLE switch is set to .5 μs. The pulse from IC1-2D is used as a sample pulse by a comparator in the word generator and sync recovery circuit.

6.32 A sample pulse of the same polarity as above is issued from IC1-2D when the SAMPLE WIDTH switch is set to one of the percent settings of the switch. The pulse width generated is that percentage of the bit interval indicated by the switch setting. Figure 6-13 shows development of the pulse. The positive going sawtooth from the voltage controlled oscillator drives slicers 2 and 3. As indicated slicer 1 is at a logical 1 during generation of the sawtooth until a certain threshold is reached at which time it reverts to a logical 0. Similarly slicer 3 is held at a logical 0 until the sawtooth reaches a certain level at which time its output changes to a logical 1 for the remaining duration of the sawtooth. During the time that both outputs are at a logical 1, a sample pulse is produced. The threshold voltages referred to above are developed through the resistor networks on CP11 which are tied in with the settings of the SAMPLE WIDTH switch.

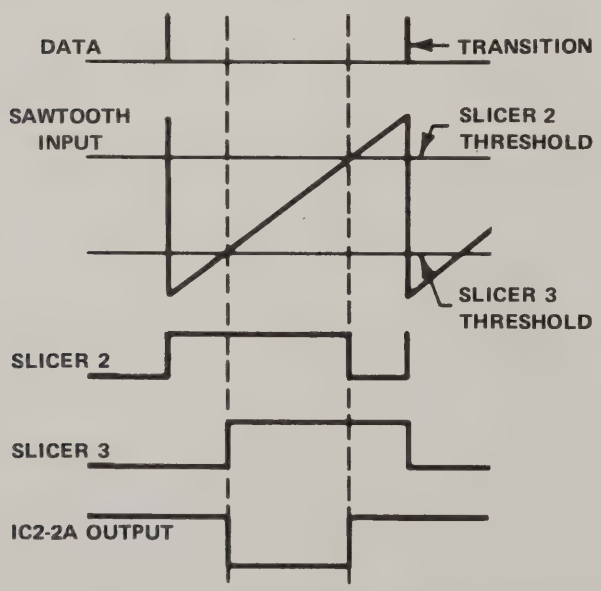


Figure 6-13. Sample Pulse Generation

6.33 The test set may be driven by an external clock signal applied to pin 20 of CP2 when the BIT RATE switch is set to EXT+ or EXT-. The limiter, lowpass filter, and slicer with feedback extending from pin 20 function in the same way as described earlier. The clock pulses are routed to the output of IC2-1C through IC2-1A or IC2-1B depending on whether the BIT RATE switch is set to EXT+ or EXT-. When the BIT RATE switch is at EXT+, the output is in phase with the input; and at EXT-, the output is 180 degrees out of phase.

6.34 Word Generator and Word Sync Recovery Circuit (Figure 6-15). The word generator generates dot signals (alternate mark and space), 63-bit quasi-random words, and 511-bit quasi-random words. The bit rate may vary from 10 to 20,000 bits per second through an external clock or through an internal clock signal.

6.35 Quasi-random words are generated by combining the clocked output of the last stage and of an intermediate stage of a shift register in an exclusive OR gate and feeding the output of the gate back to the first stage of the register (Figure 6-14). If the outputs of the stages are the same, the output of the gate will be a logical 1 and if different a logical 0. With each clock pulse the contents of the register are shifted to the right and the output of the exclusive OR gate is deposited in the first stage. Depending on the selection of an intermediate stage of a b-staged register, a repetitive train with a period of 2±-1 bits may be generated having qualities similar to a randomly selected digit.

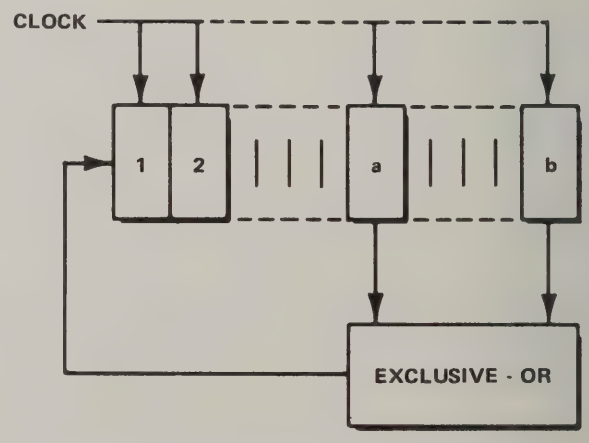


Figure 6-14. Quasi-Random Word Generation

6.36 In generating a 63-bit word six stages are required with the fifth stage serving as the intermediate stage while for a 511-bit word nine stages are required with the fifth stage again serving as the intermediate stage (Figure 6-15). Gates IC1-3D, IC1-3A, IC2-4A, IC1-3C, IC2-3A, and IC2-3C make up the exclusive OR gate with gate IC2-3C acting as the last stage. A particular setting of

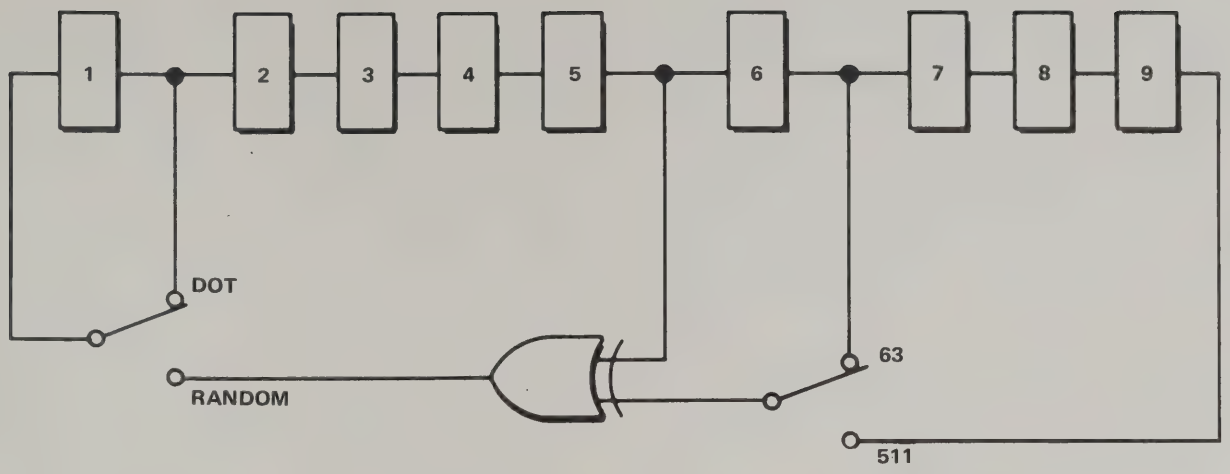


Figure 6-15. Word Switching Function

the WORD LENGTH switch conditions these gates for the desired word length. The setting of the WORD LENGTH switch is also used to condition gates IC12D or IC2-3C in the selection of one of the multibit words or a dot signal. Dot signals are generated through feedback from the output of the first stage of the resister so that the first stage acts as a binary counter.

6.37 Under data transmit conditions the TEST SET MODE switch is set to one of the TRMT positions and a ground is applied to the C input of FF3-2. The resulting logical 0 from the set output of the flip flop disables gates IC1-2C and IC1-2A causing their outputs to be locked to a logical 1. Also, if the WORD SYNC switch is in its OFF position, the S input of FF3-1 is at a logical 1, and with the C input of the flip flop operating at the clock rate, the set output of the flip flop is at a logical 0 causing G3-7 to become disabled and its output locked at a logical 1. Under all of the above conditions gates IC1-2B, IC2-1C, and IC1-3B are conditioned to route the word or dot signal from IC1-2A back to the shift register.

6.38 The word or dot signal from IC1-2A is also routed to output amplifier Q6 which provides a ±4 volt or a ±0.7 volt bipolar signal depending on the setting of the SIGNAL LEVEL switch. The signal is then processed by other circuits depending on the position of the TEST SET MODE switch.

6.39 The clock signal is routed from the clock circuits through buffer IC3-1B to the shift register. For negative transition at the T input of each stage the register advances in response. The clock is in synchronism with received data in the receive mode. Clock signal phase is such that transitions of the locally produced word are coincident with the mean of the transitions of the received later signal.

6.40 Data signals received on the RDI lead to IC1-1C and IC2-2B of a comparator consisting of IC1-1C, IC2-2A, and IC2-2B are compared with the word generator output of IC1-2A when the positive sample pulses (described under clock circuits) appear on the SP lead to IC2-2A and IC2-2B. If a word generator and incoming data signal do not agree at the input of IC1-1C flip flop FF3-2 is set and a logical 0 is sent to the error counting circuit through lead P. FF3-2 is reset during the negative excursion of a clock pulse by way of the C3, CR6, and R8 combination. Figure 6-16 shows the relationship between the pulses.

6.41 The Q1, Q10 clock detector senses excursions of the clock signal at the output of IC3-1B and operates lamp driver Q2 to light the NO CLOCK lamp when no clock signal is present. Similarly the Q7, Q8, Q11 data

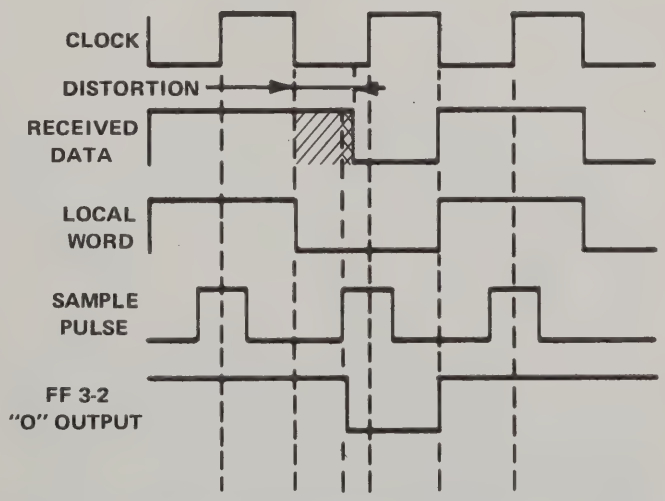


Figure 6-16. Comparator Operation

detector drives the Q9 lamp driver to light the NO DATA lamp when there is no data signal on the RDI lead in the receive mode of operation or no data input to IC5-1 of the shift register in the transmit mode.

6.42 **Error Counter Circuit (Figure 6-22).** A bit error detected by the comparator in the word generator and sync recovery circuit is routed as a logical 0 on the CG lead flip-flop IC5-1 (Figure 6-22). The flip-flop is thereby set and the resulting logical 1 is applied to IC2-1A. The other two inputs to IC2-1A are at a logical 1 when the COUNTER switch is set to the BIT ERRORS position and the resulting low from IC2-1A is used to drive the decade counter. With the J and K inputs tied to ground and +5 volts, a negative excursion of the clock signal detected on the DD lead to FF4-4 resets the flip flop.

6.43 With the COUNTER switch set at one of the BLOCK ERRORS positions, a single error within a block containing one or more errors will trigger IC5-1 for an error count. A block contains 1, 2, 4, 8, or 16 times the length of a 63 or 511 bit words depending on the setting of the COUNTER switch. In the BLOCK ERRORS position, FF4-4 is reset at the end of a block interval by a negative synch pulse from one of the IC7-1A, IC7-1B, IC7-2A, or IC7-2B binary counters associated, respectively, with one of the 2WL, 4WL, 8WL, or 16WL BLOCK ERROR positions of the COUNTER switch rather than by a negative excursion of a clock pulse. Each successive counter divides the word sync pulse rate received on the R lead to the T input of IC7-1A by 2 to obtain the 2, 4, 8, and 16-word intervals.

6.44 The capacity of the decade counter is to register a count of 99. A count of 100 resets the counter to 00 and triggers the Q1, Q2 single shot. The output of the single shot sets flip flop Q3, Q4 which drives amplifier Q5 to cause the LAMP OVERFLOW lamp to light. Depressing the RESET button causes the flip flops in the error and interval counter circuit to be cleared and the overflow lamp to go out.

6.45 **Interval Counter Circuit (Figure 6.22).** The interval counter circuit provides a means of determining the sequence of arrival of two incoming signals and the measurement of the time interval between their arrivals. Alternatively, it provides measurement of the duration of a pulse.

6.46 During tests connections are made through the TP1 and TP2 points on the program matrix or front panel, and the COUNTER switch is set to one of the INTERVAL positions. Signals to be measured may be positive or bipolar voltages and contact closures. Positive signals applied to input amplifiers Q1.2 and Q1.3 are inverted by the amplifiers and again inverted, respectively, by IC1-2A and IC1-2B. Flip flops FF4-1 and FF4-2 are both set by negative trigger inputs at the S connection of each flip flop. The negative triggers are formed, respectively, by differentiators C3-R1 and C4-R12. If it is desired to have the negative going leading edge of a signal differentiated, the TRIGGER switch should be set to +/OPEN thereby necessitating another inversion (via IC2-2B or IC1-2C) of the original signal to the input amplifier. If it is desired to have the trailing edge of a negative going signal differentiated the switch should be set to -/CLOSE.

6.47 If in the determination of the sequence of arrival of two signals, the first signal should arrive at TP1 first, FF4-1 will be set by the differentiated signal. The set output will then gate IC1-2D to set FF4-3. This in turn will gate B1 to activate the lamp driver and turn the FIRST TP1 lamp on. If the signal first to arrive is at TP2, B2 will be gated by the set output of FF4-2 resulting in the turn on of the FIRST TP2 lamp.

6.48 When the first signal to arrive sets either FF4-1 or FF4-2, the decode counter will be enabled through gates IC1-1A, IC2-1C, IC2-1B, and IC2-1A. The arrival of the second signal will disable IC1-1A thereby disabling the counter which then displays the time interval elapsed.

6.49 For purposes of accommodating the four interval ranges and obtaining the desired degree of resolution, the clock frequencies are set at frequencies of 10, 100, 1K, and 10 kHz. Selection of a particular frequency is set through the INTERVAL positions of the COUNTER switch. Capacitors affecting the frequencies are located on CP10 and CP14 (See Figure 6-20).

6.50 **Parallel Data Transmit Circuit (Figure 6-23).** The transmit clock Q4, Q5 is a free running multivibrator providing an asymmetric, 75-Hz output to drive flip-flops FF5-1 and FF5-2 and the clock output amplifier Q10. The flip-flops change state with negative excursions of the clock output. FF5-1 provides a dotting signal to the timing channel through C1D9, and FF5-2 provides a dotting signal for the eight data channels through C1D1 through C1D8. Alternatively, the data channels may receive the pseudo-random word output from the word generator through the DOI lead.

6.51 The outputs of both FF5-1 are in phase when the TRMT CLOCK PHASE switch is set to NOR. When the switch is in the ADV or RET position, the phase of the clock signal at the output of Q10 is advanced or retarded, respectively, 1.5ms with respect to the data signal at the logical 1 output of FF9-2. Gate GA is used to promote the time phasing. When the TEST SET MODE switch is in the TRMT 402 position and the BIT RATE switch is set to EXT+, the Q10 clock output is routed to the timing channel of the clock circuit through the EC lead.

6.52 When the TEST MODE switch is set to one of the eight channel positions, the word generator output coming in on the DOI lead is routed through the respective CID output to the J3 connector driver. The dot signal from FF5-2 is then connected through the TEST MODE switch to the seven other output drivers to the J3 connector.

6.53 Individual or simultaneous testing may be accomplished when the TEST MODE switch is set to ALL RDM, the word generator output being connected to all eight output drivers. When the switch is in the ALL DOT position, the dot output of FF5-2 is connected to all drivers. In the ALL SPC position, a constant-12 volt space signal is provided for all eight drivers. Contact closure type of operation is provided by the drivers.

6.54 Parallel Data Receive Circuit (Figure 6-24). Incoming data signals come in to the test set through pins 2 through 10 except pin 6 of J4 serving the eight data channels, and the timing signal comes in through pin 6. Testing may be accomplished on an individual channel basis or all tests may be performed simultaneously, depending on whether the setting of the TEST MODE switch is at one of the channel positions or at the ALL RDM position.

6.55 The received timing signal on pin 6 of J4 is routed through the Q2.10, Q3.10 level converter to the clocking input on the EC lead of the clock circuit (Figure 6-20) after being routed to the TEST SET MODE switch on the RC lead (Fig. 6-23). The level converter prevents contact bounce type of behavior on contact closure type operations. Data signals which are tested on an individual channel basis are routed through level converter Q2.9, Q3.9 and through the TEST SET MODE switch when that switch is set to RCV 402 to the receive data DI lead of the clock circuit (Figure 6-20). The data signal is checked for errors by the comparator circuit in the word generator and word sync recovery circuit as in the serial mode of operation (paragraph 6-40).

6.56 When all channels are being tested simultaneously, the TEST SET MODE switch is set to ALL RDM, and the pseudo-random word imposed on all channels is routed to an error detector consisting of Q1, GB, GC, Q11, Q2, and exclusive OR gate Q3. There, comparison is made with the locally generated pseudo-random word coming in on the LW lead to Q1.

6.57 The locally generated word is inverted by Q1 and compared with the incoming signals in gates GB and GC. Gate Q1 provides for the inverting effect of contact closure, since a logical 1 from the transmitting test set word generator is inverted to ground by the output drivers at that end. Therefore, in an error-free situation, a logical 1 generated by the local word generator is inverted to a logical 0 and fed to gates GB and GC along with the zeros on all eight other channels. This causes both inputs to exclusive OR GATE Q3 to be the same. The resulting low or logical 0 from Q3 causes the output of the Q2.9, Q3.9 level converter to go high. The logical 1 is routed to the receive DI lead in the clock circuit where it is then routed to the comparator in the word generator and sync recovery circuit. Since there is agreement at the comparator between the locally generated word and eight channel transmitted words, no error is detected.

6.58 Reference Voltage (See Figure 6-25). With the REFERENCE VOLTAGE OUTPUT switch set to TP3, reference voltages of +7.0, ±2.0, ±1.0, and ±.477 volts are available at TP3 through the selective setting of the SELECT switch. Selection of an additional ADJ position of the SELECT switch provides a variable voltage of 0 to +8 volts at TP3 through adjustment of the ADJUST control. Zener diode CR1 and R30 or R31, depending on polarity, provide a reference voltage of plus or minus 8.2 volts.

6.59 Meter Circuit (See Figure 6-26). Through the meter circuit ac and dc voltage and resistance may be measured, and low-level audio signals may be monitored. When the FUNCTION switch is in the VOLT INT position, the dc voltages on the 25 vertical buses in the program matrix may be monitored through the 25 position VERTICAL MONITOR switch. Connections are made to the external INPUT jacks when the FUNCTION switch is set to the VOLT/OHM EXT or SPEAKER for measurements or monitoring.

6.60 When the meter circuit is used as a dc voltmeter, the meter sensitivity is 20,000 ohms per volt. Resistors R1 through R4 provides full-scale ranges of 1, 3, 10, and 30 vdc. The POLARITY switch provides the convenience of reversing the leads to the meter. The red jack is designated as the positive terminal when the switch is in the NORMAL position.

6.61 A somewhat simplified representation of the meter circuit when used as an ohmmeter is shown in Figure 6-17. The meter is provided with two ranges having midscale readings of 100 and 10,000 ohms for respective RANGE switch settings of X1 and X100. R33 is the ZERO OHMS adjustment for the meter.

6.62 Figure 6-18 is a somewhat simplified presentation of the ac voltmeter circuit. The circuit has the capability of measuring voice frequency signals over five full scale ranges ranging from 10 millivolts to 1 volt. Incoming signals are applied through isolation transformer T1, and except for the 10 millivolt range, applied through one or more attenuating resistors depending on the RANGE setting of the meter. Capacitor C1 blocks dc current permitting direct connection to a telephone line. CR6,

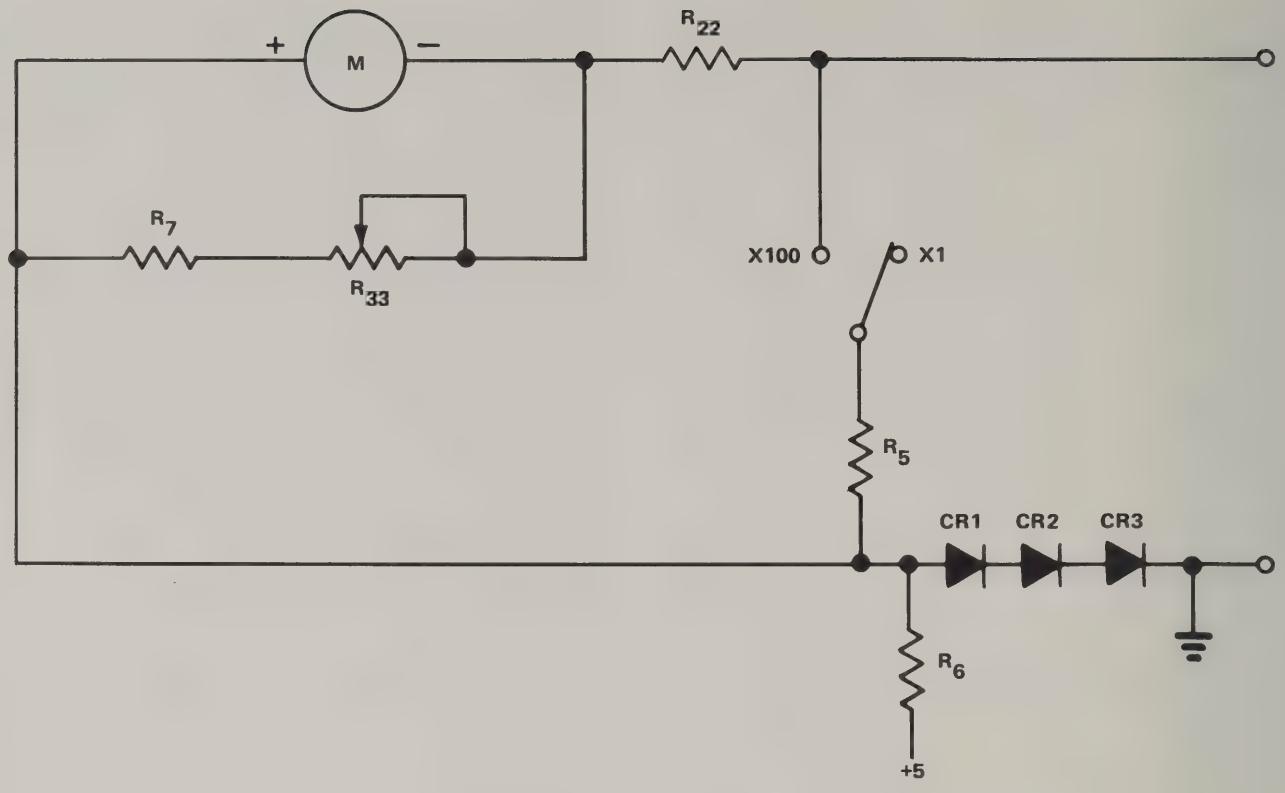


Figure 6-17. Ohmmeter

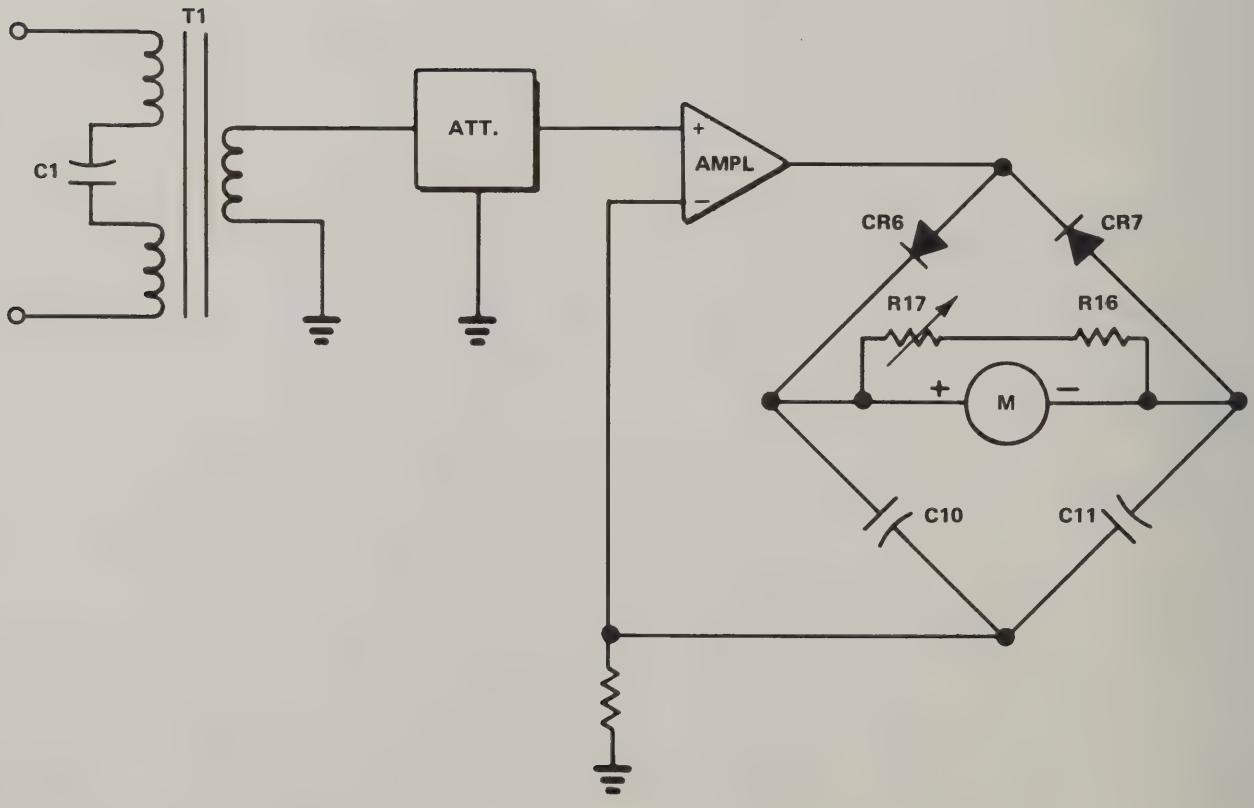


Figure 6-18. AC Voltmeter Circuit

CR7, C10, and C11 comprise a bridge rectifier which provides a feedback voltage across the resistor connected to the lower terminal of the amplifier which is proportional to the alternating current being rectified. The net effect of this is to keep the dc meter current proportional to the input voltage despite nonlinearities in CR6 and CR7. The ac meter scale is calibrated in RMS values for sine waves. Shunts 16 and R17 across the meter are used for calibration purposes.

6.63 For audio monitoring of the ac line signal the FUNCTION switch is set to the SPKR position. Input is only through the red and black jacks (TP4 and TP5) on the front panel. Volume control is provided through the ACV positions of the RANGE switch. R11 controls the gain of the feedback amplifier. Additional gain for the speaker output is provided through the speaker amplifier Q1.

6.64 When the FUNCTION switch is in the OFF position, the meter movement is short circuited. This provides an important damping effect on the movement which is especially significant when the test set is being transported.

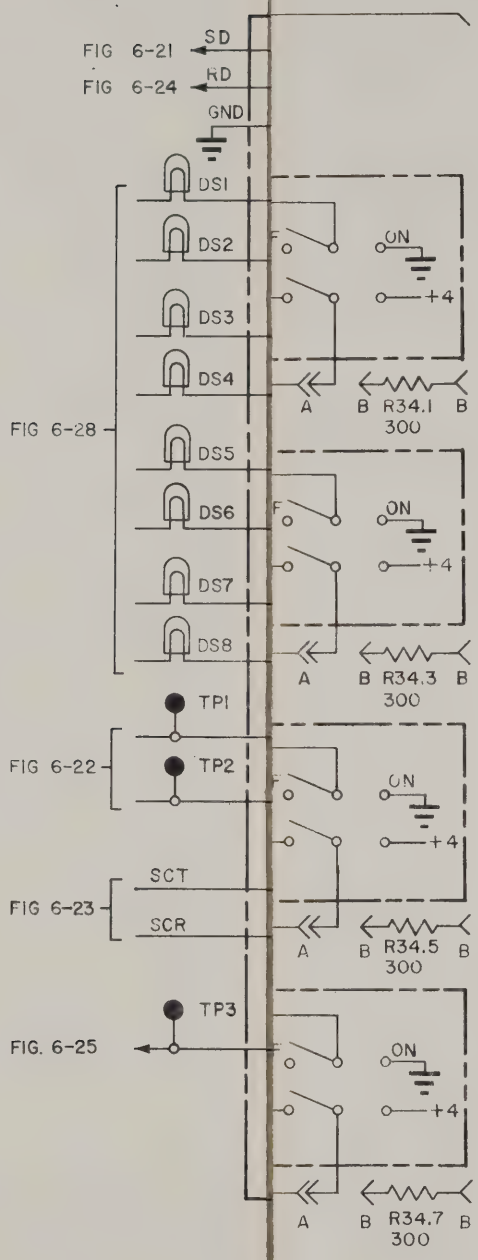
6.65 **Power Supply (Figure 6-27).** The power supply provides regulated outputs of +5 and ±12 volts and unregulated outputs of +23 and +200 volts. Nominal input power is 115 Vac, 60 Hz.

6.66 Power is applied to the T1 primary through F1 and the POWER switch/lamp. One secondary develops opposite phase voltages with respect to ground of 18 Vac (7-5 and 3-5) and 9 Vac (6-5 and 4-5). Another secondary provides 160 Vac which is rectified by CR1 and C1 in conjunction with bleed resistor R1 to provide 200 Vdc for operation of the decade counter display tubes.

6.67 CR2 and CR4 in conjunction with C1 rectify the voltage for the +12 volt supply while CR3 and CR5 in conjunction with C2 rectify the voltage for the -12 volt supply. CR10 and CR11 in conjunction with C3 rectify the voltage for the +5 volt supply. The rectified and filtered voltage for the +12 volt supply is at a +23 volt level before regulation and is tapped off through F2 for operation of the test set lamps.

6.68 The regulators set the actual level of the dc voltages, reduce ripple, and maintain the voltages at a constant level despite variations in the line voltage and load current. Zener diodes CR6, CR9, and CR7 set the reference voltage levels respectively for the +12, -12, and +5 power supplies. These diodes also reduce ripple because of their low dynamic impedance. The unregulated voltages are applied to series regulators operating in a common collector configuration thereby providing a low impedance output. The Q1-Q1 and Q3-Q2 compound connections perform as high gain power transistors.

6.69 The +5 volt supply output may be varied over a limited range through the various voltage divider arrangements of R13 and R9 in combinations with R10, R11, and R12. Integrated circuits in the +5 volt supply are protected against overvoltage by a crowbar circuit consisting of CR8, R16, R17, R15, C4 and Q3. If the voltage of the power supply should exceed +5.4 volts, zener diode CR8 will conduct causing silicon controlled rectifier Q3 to conduct. The resulting heavy current through F5, Q3, and R15 will cause F5 to blow.



NOTES

1. RESISTORS (R1) THRU (R25) ARE 300K.
2. RESISTORS (R1) THRU (R25) ARE MOUNTED BETWEEN SECTION 1 (FRONT & REAR) AND DUMMY SECTION 2 OF S29.
3. THE PROGRAM MATRIX IS PROGRAMMED AS REQUIRED USING PROGRAM PINS P1, P2 and P3.
4. SERIAL NUMBERS 101-361 WILL HAVE OPTION A' UNLESS MODIFICATION KIT 2924B-M1 IS INSTALLED
   SERIAL NUMBERS 362 AND UP WILL HAVE 1914B-M1 FACTORY INSTALLED
5. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS' CAPACITANCE VALUES ARE IN MICROFARADS' VALUES PRECEDED BY THE SYMBOL + (PLUS) OR – (MINUS) ARE IN VOLTS.
6. ⏚ GROUND RETURN.

Figure 6-19. Interface Connections

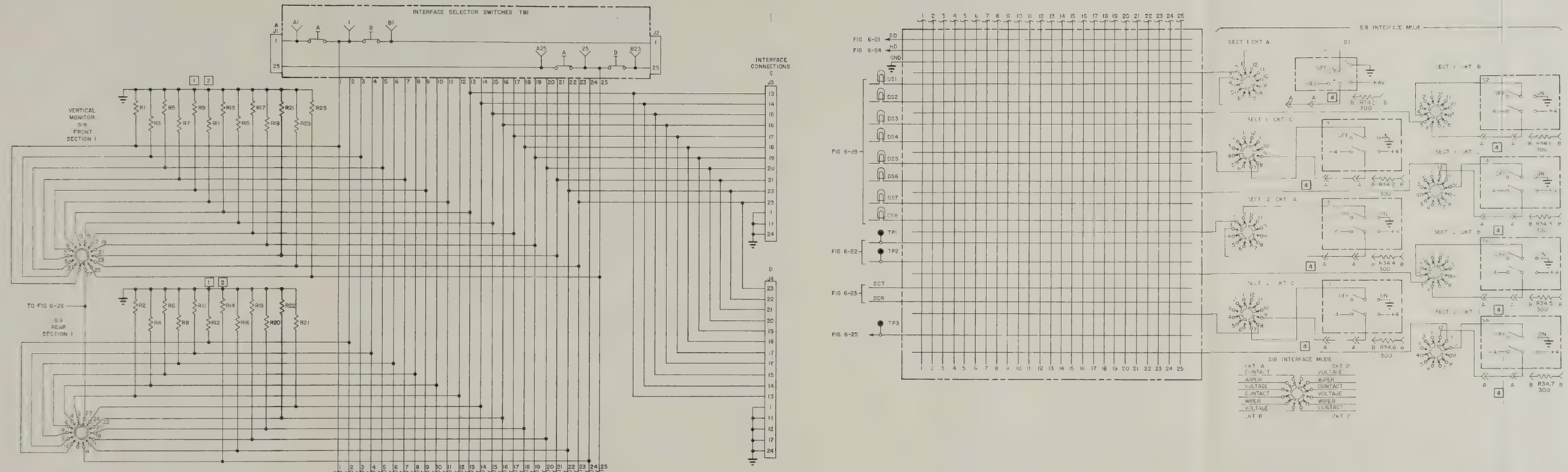


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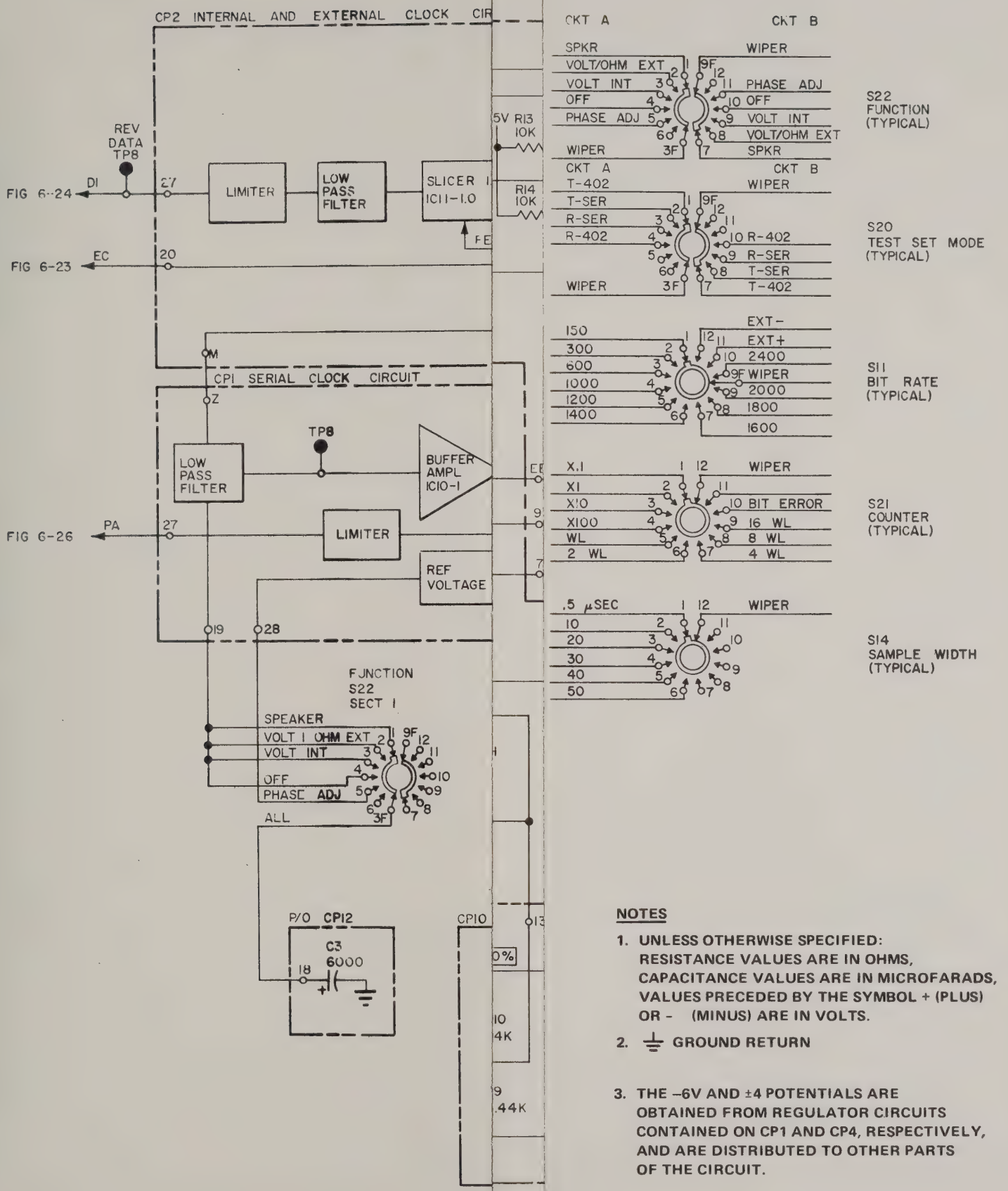
Figure 6-19. Interface Connections



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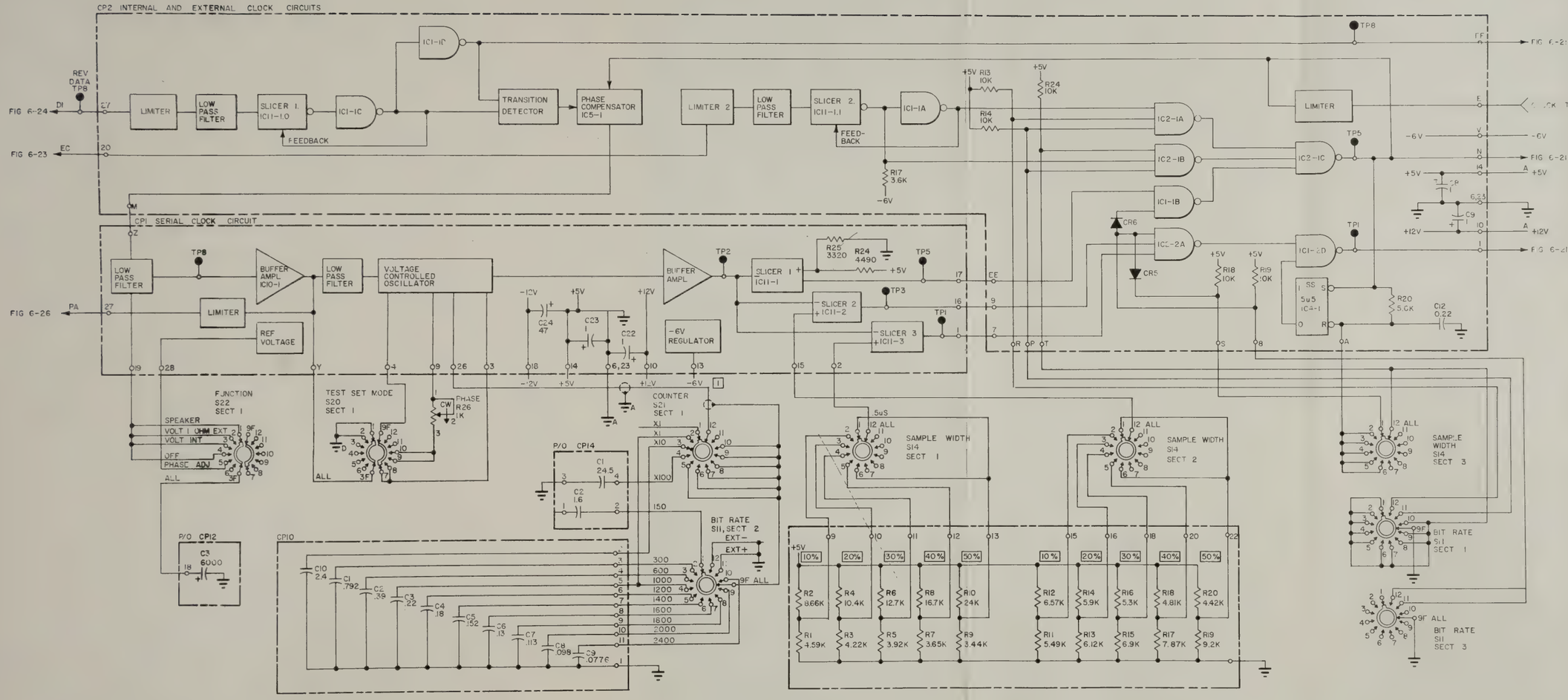
2. ⏚ GROUND RETURN
3. THE –6V AND ±4 POTENTIALS ARE OBTAINED FROM REGULATOR CIRCUITS CONTAINED ON CP1 AND CP4, RESPECTIVELY, AND ARE DISTRIBUTED TO OTHER PARTS OF THE CIRCUIT.

Figure 6-20. Clock Circuit



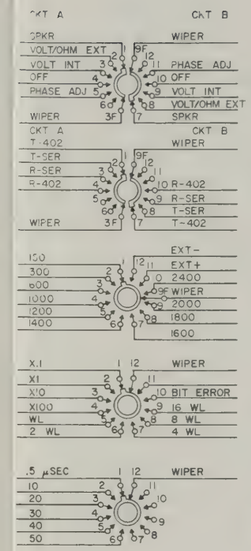


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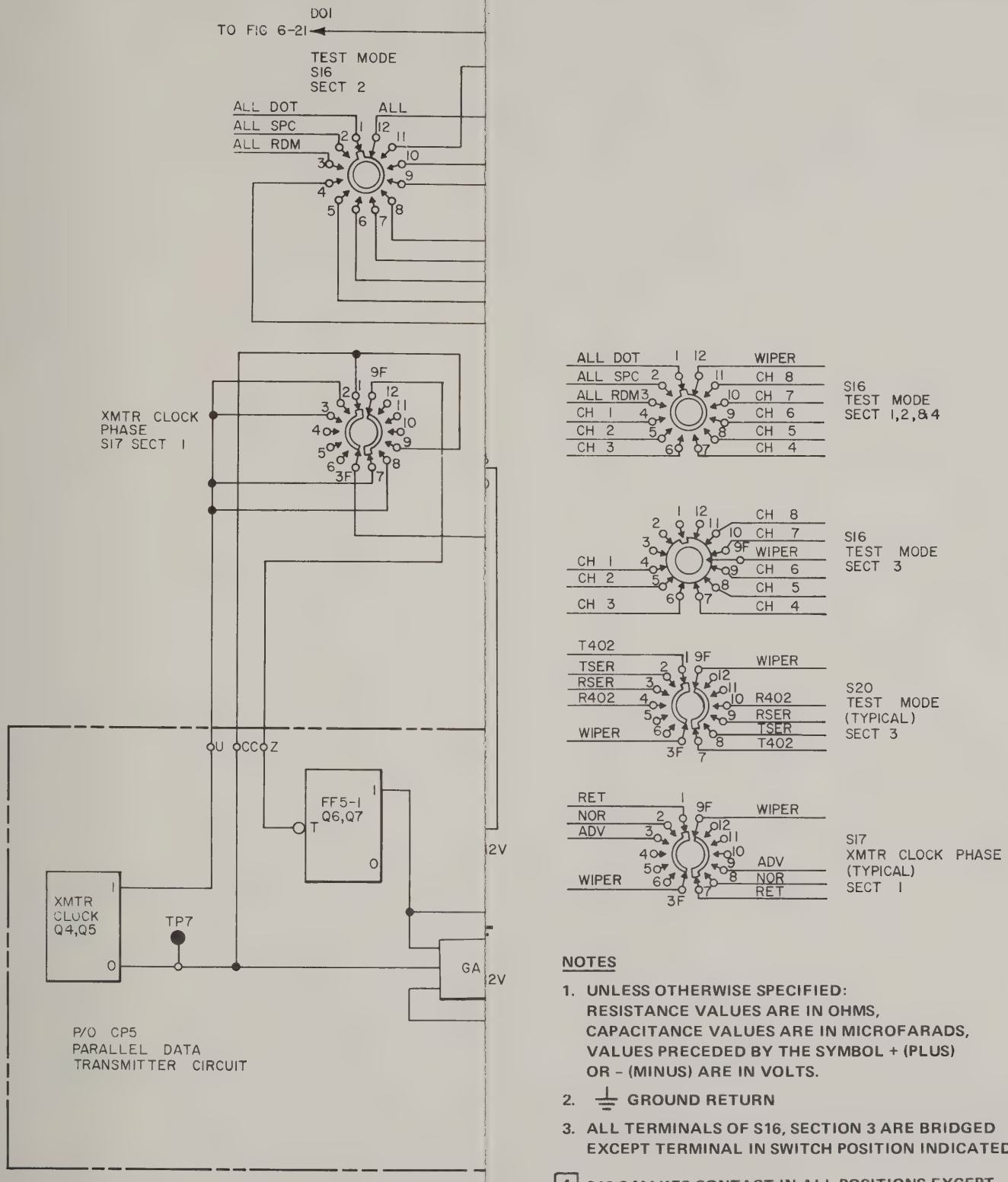
Figure 6-20. Clock Circuit



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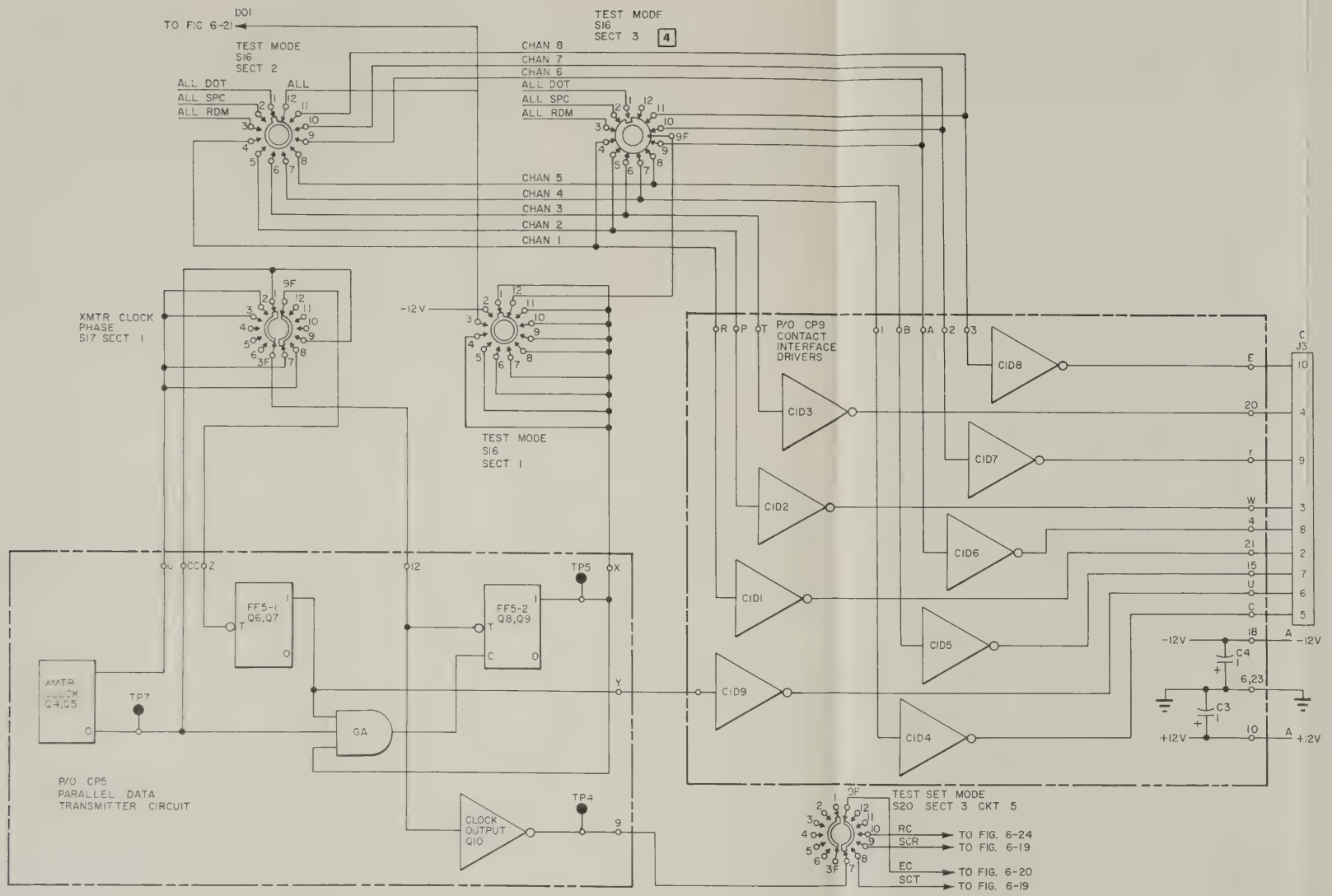
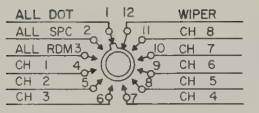
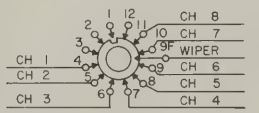
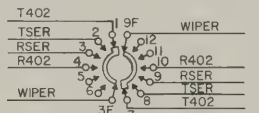
2. ⏚ GROUND RETURN
3. ALL TERMINALS OF S16, SECTION 3 ARE BRIDGED EXCEPT TERMINAL IN SWITCH POSITION INDICATED
4. S16-3 MAKES CONTACT IN ALL POSITIONS EXCEPT THE INDICATED POSITION.

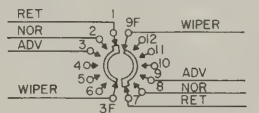
Figure 6-23. Parallel Data Transmit Circuit









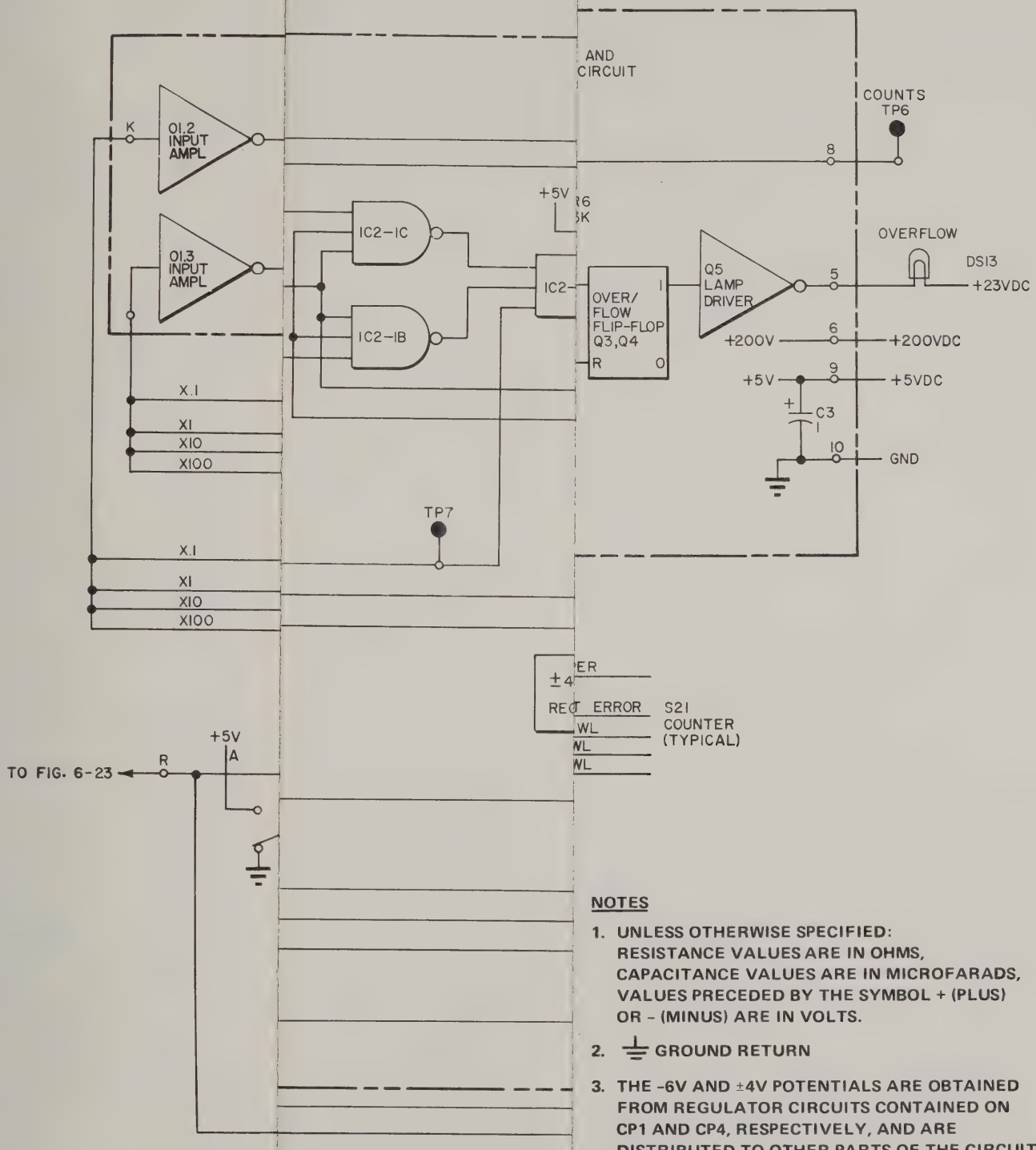


NOTES

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. ALL TERMINALS OF S16, SECTION 3 ARE BRIDGED EXCEPT TERMINAL IN SWITCH POSITION INDICATED

[4] S16-3 MAKES CONTACT IN ALL POSITIONS EXCEPT THE INDICATED POSITION.

Figure 6-23. Parallel Data Transmit Circuit



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. THE -6V AND ±4V POTENTIALS ARE OBTAINED FROM REGULATOR CIRCUITS CONTAINED ON CP1 AND CP4, RESPECTIVELY, AND ARE DISTRIBUTED TO OTHER PARTS OF THE CIRCUIT.

Figure 6-22. Error and Interval Counter Circuit

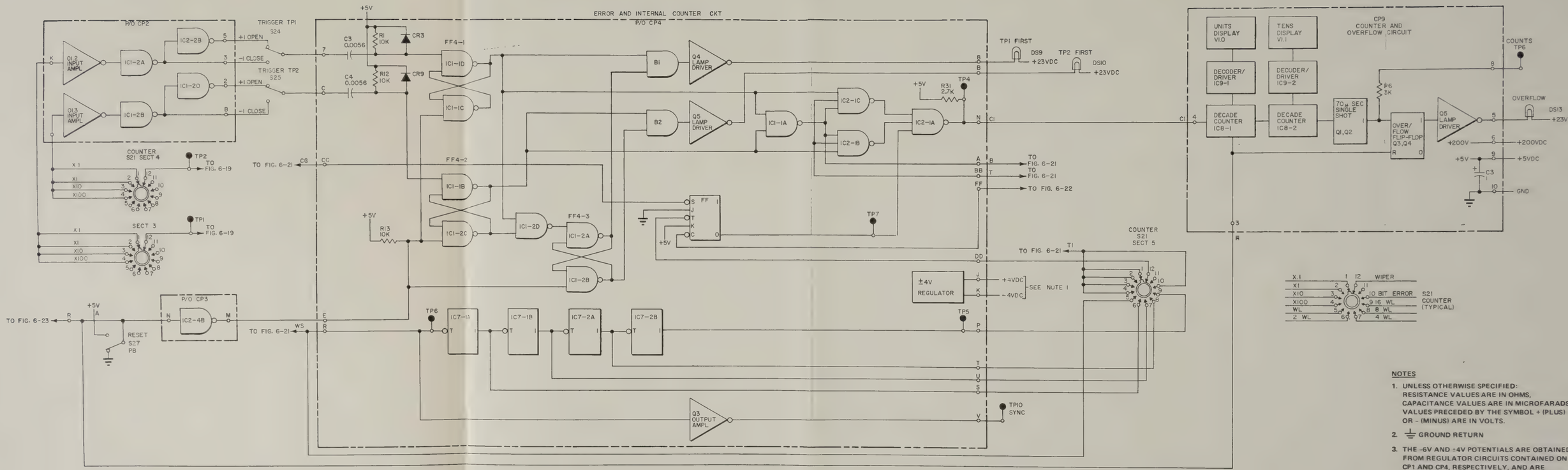


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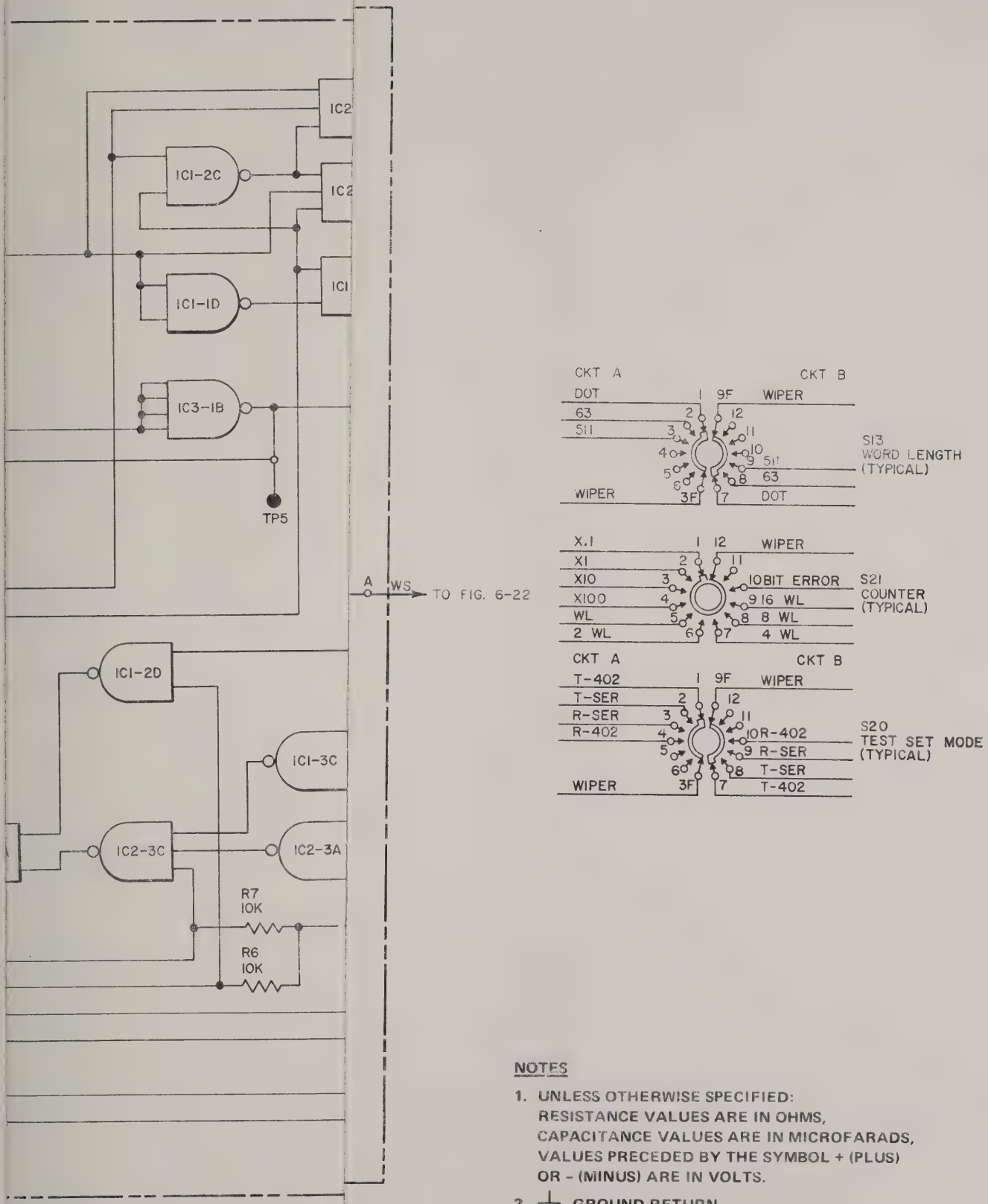
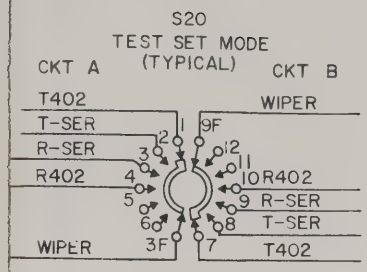
Figure 6-22. Error and Interval Counter Circuit



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN

Figure 6-21. Word Generator and Word Sync Recovery Circuit



12VDC

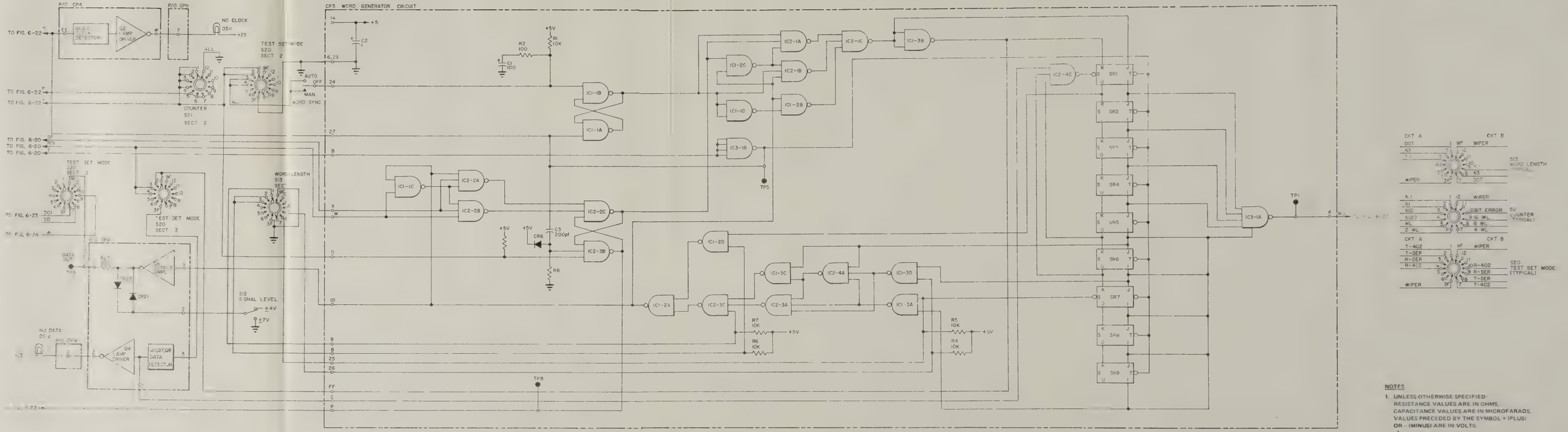
ND

12VDC

NOTES

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN

Figure 6-24. Parallel Data Receive Circuit



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS.
   CAPACITANCE VALUES ARE IN MICROFARADS.
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2. ⏚ GROUND RETURN

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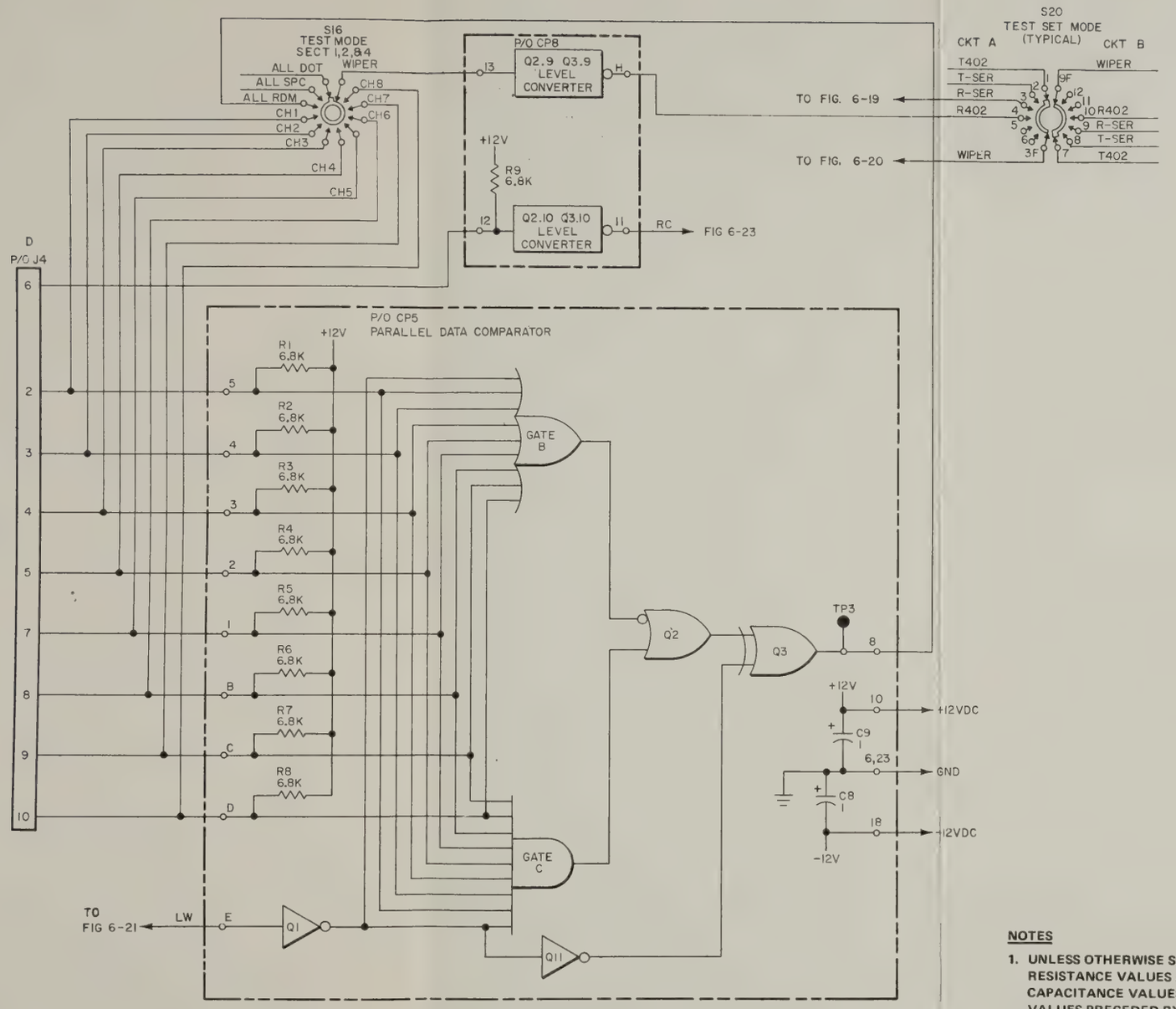

NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
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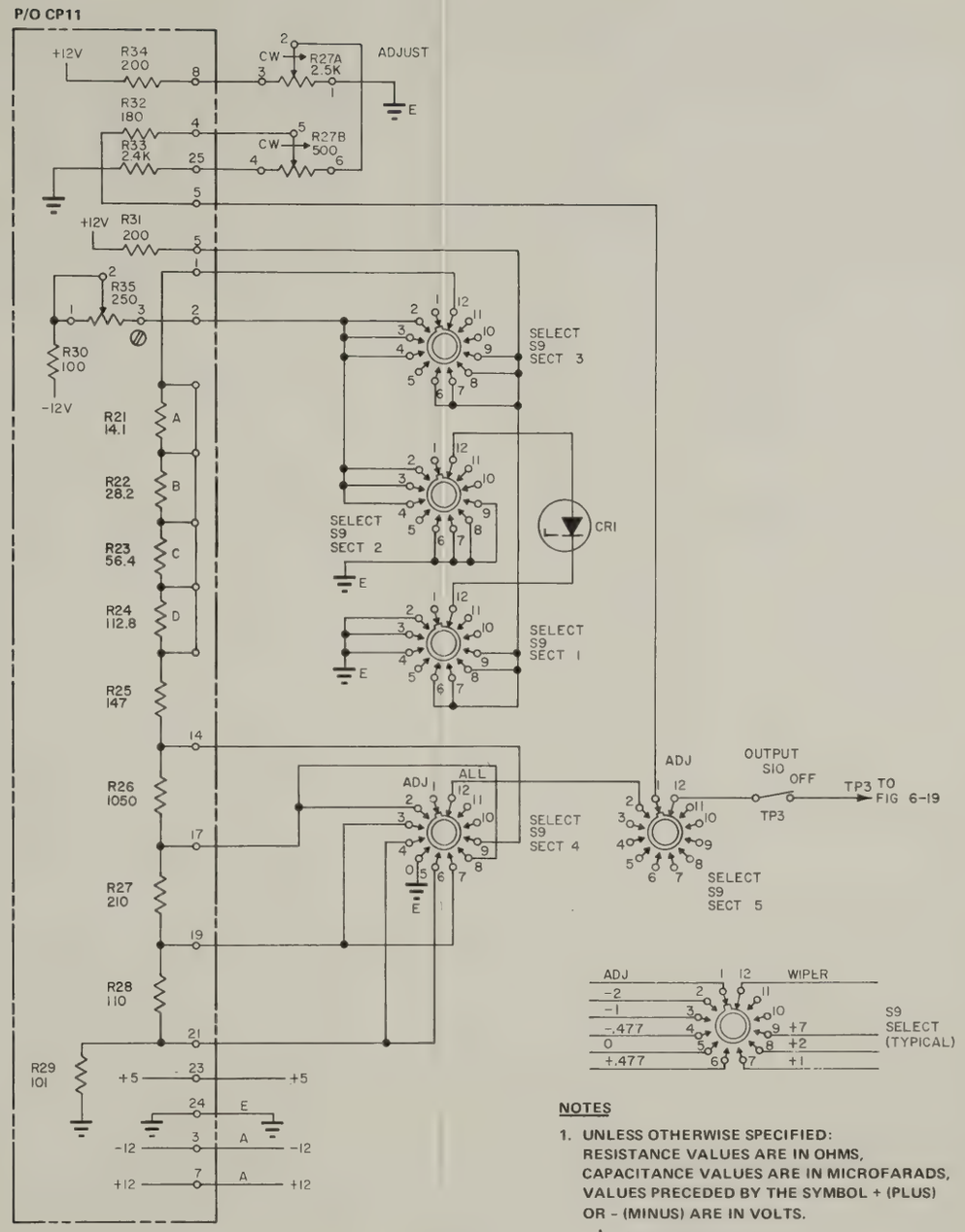
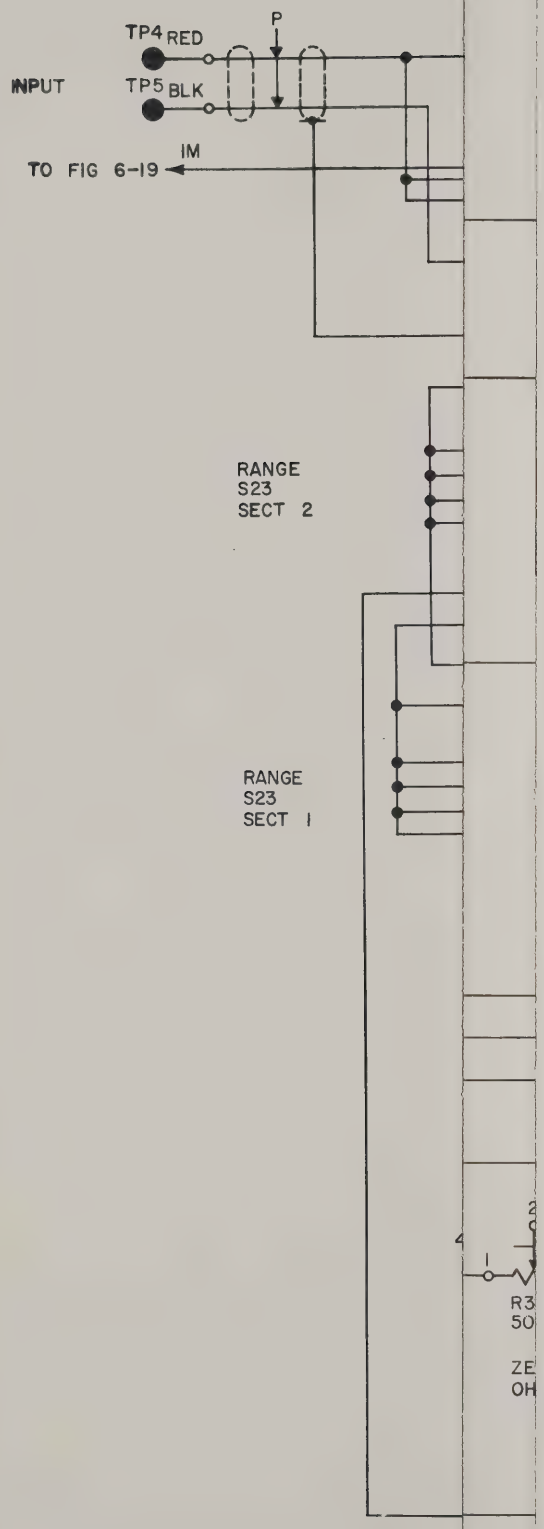


NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN

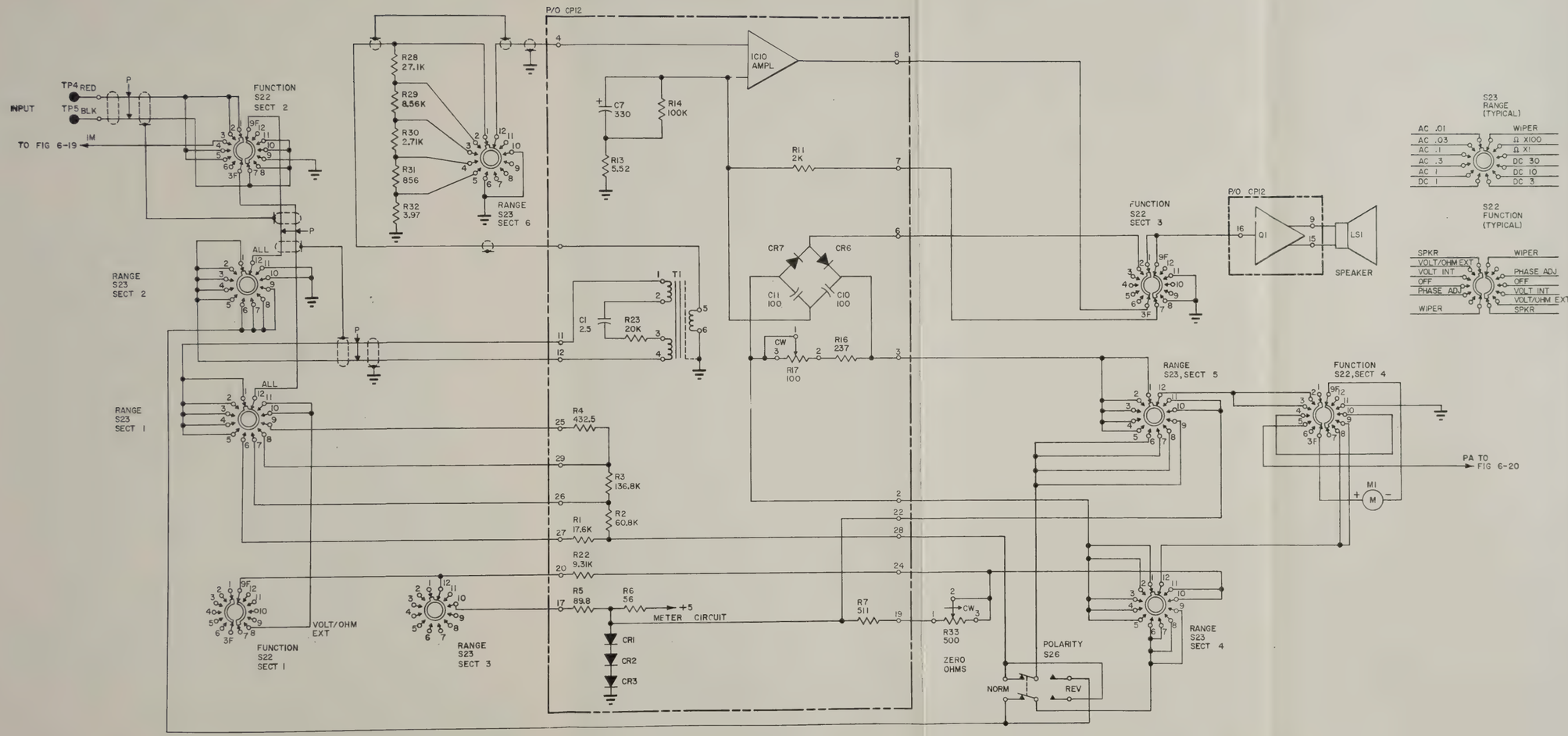
Figure 6-25. Reference Voltage Circuit



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN

Figure 6-26. Meter Circuit



NOTES

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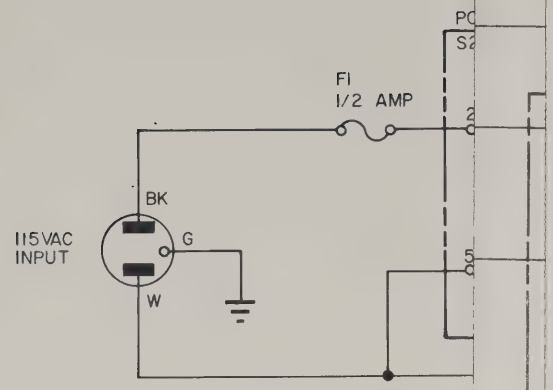
2. ⏚ GROUND RETURN

Figure 6-26. Meter Circuit



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFA VALUES PRECEDED BY THE SYMBOL + (P OR – (MINUS) ARE IN VOLTS.
2. THE GROUND TERMINALS OF CAPACITO AND C3 SHALL BE INTERCONNECTED AN TO A COMMON GROUND POINT AT OR IN ATE VICINITY OF, TERMINAL 5 OF T1 US WIRE. PIN 20 OF CP11 AND THE FRAME G SHALL BE CONNECTED TO THE COMMON POINT WITH 160A WIRE. ALL REMAININ SHALL BE 206A, OR LARGER.
3. STRAPS A, B, AND C ARE CUT AS NECESS THE +5V SUPPLY TO 4.75 ±0.05V. IF SUPPLY IS NOT WITHIN LIMITS, REINS STRAPS, A THROUGH C AND MEASURE V IF THE CROWBAR CIRCUIT BLOWS F5, TE REMOVE ALL LEADS FROM CP13 PINS 26 EXCEPT FOR THE COLLECTOR LEAD OF MOUNTED Q3, AND TEMPORARILY SHOR WHILE MAKING ADJUSTMENT.

IF VOLTMETER READS BETWEEN:	CUT STRAP
4.70 – 4.80	None
4.81 – 4.84	A
4.85 – 4.91	B
4.92 – 4.98	A,B
4.99 – 5.05	C
5.06 – 5.12	A,C
5.13 – 5.19	B,C
5.20 – 5.26	A,B,C

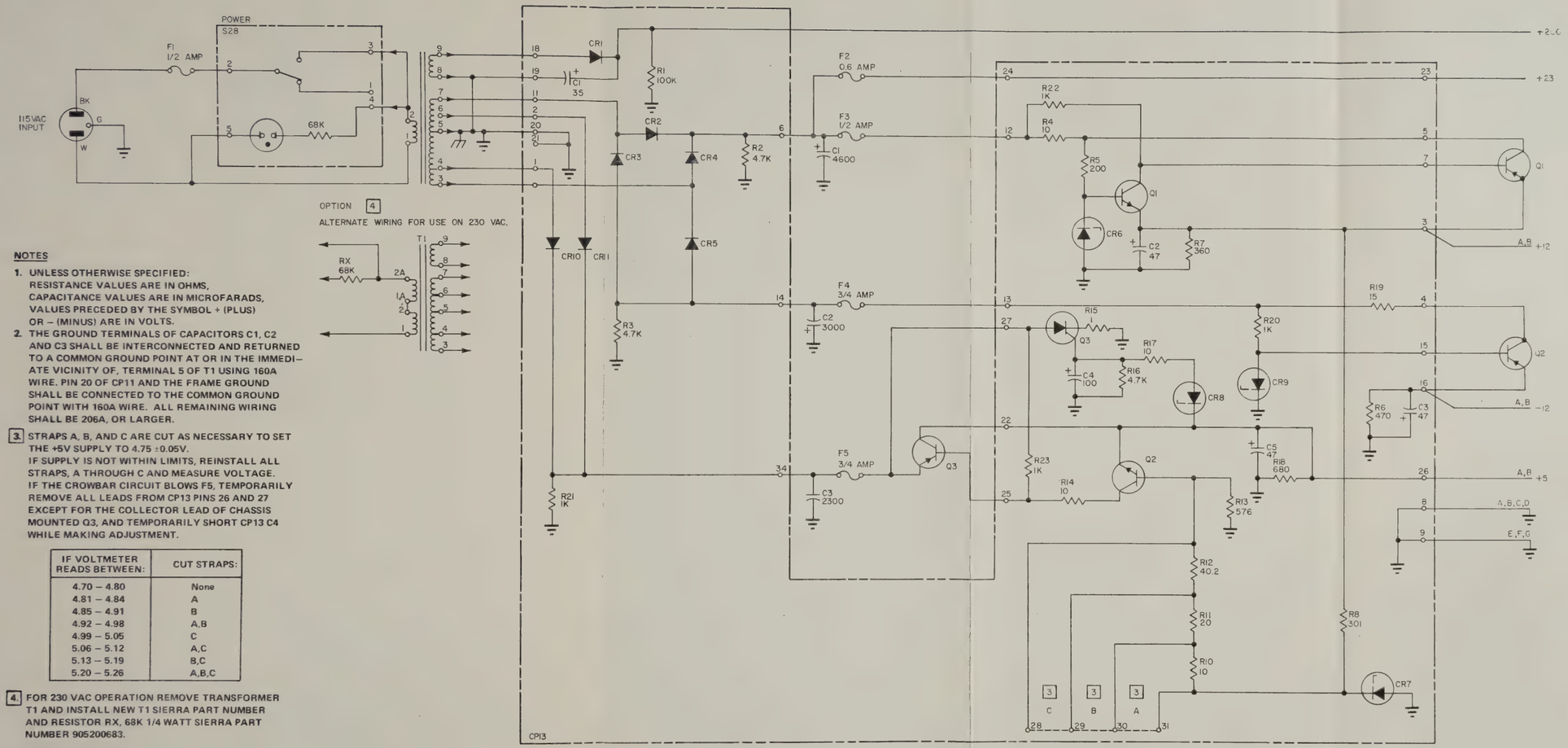
4. FOR 230 VAC OPERATION REMOVE TRA T1 AND INSTALL NEW T1 SIERRA PART AND RESISTOR RX, 68K 1/4 WATT SIERR NUMBER 905200683.

VOLTAGE CHART

TAKEN USING A 20 KΩ/VOLT DC, ETER.

E	B	C	CATHODE	ANODE	GATE	
1.0	20.8	11.8	To protect the logic CX Integrated Circuits, remove all leads from CP-13 pins 26 & 27 except the collector lead of chassis-mounted Q3. This is very important if the +5V crowbar circuit is inoperative			
1.3	-11.5	-21.8				
0.9	10.6	4.75				
1.8	12.2	20.8				
4.8	5.6	10.6				
			0.0	10.9	0.0	
			225	200Vac		Readings taken with fuses F2, F3, F4 pulled.
			27	20Vac		
			20Vac	-27		
			27	20Vac		
			20Vac	-27		
			12.2	0		
			6.9	0		
			4.8	0.3		
			0	-11.4		
			13V	10Vac		Readings taken with F5 pulled.
			13V	10Vac		

Figure 6-27. Power Supply



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR – (MINUS) ARE IN VOLTS.
2. THE GROUND TERMINALS OF CAPACITORS C1, C2 AND C3 SHALL BE INTERCONNECTED AND RETURNED TO A COMMON GROUND POINT AT OR IN THE IMMEDIATE VICINITY OF, TERMINAL 5 OF T1 USING 160A WIRE. PIN 20 OF CP11 AND THE FRAME GROUND SHALL BE CONNECTED TO THE COMMON GROUND POINT WITH 160A WIRE. ALL REMAINING WIRING SHALL BE 206A, OR LARGER.

[3] STRAPS A, B, AND C ARE CUT AS NECESSARY TO SET THE +5V SUPPLY TO 4.75 ±0.05V.
IF SUPPLY IS NOT WITHIN LIMITS, REINSTALL ALL STRAPS, A THROUGH C AND MEASURE VOLTAGE.
IF THE CROWBAR CIRCUIT BLOWS F5, TEMPORARILY REMOVE ALL LEADS FROM CP13 PINS 26 AND 27 EXCEPT FOR THE COLLECTOR LEAD OF CHASSIS MOUNTED Q3, AND TEMPORARILY SHORT CP13 C4 WHILE MAKING ADJUSTMENT.

IF VOLTMETER READS BETWEEN:	CUT STRAPS:
4.70 – 4.80	None
4.81 – 4.84	A
4.85 – 4.91	B
4.92 – 4.98	A,B
4.99 – 5.05	C
5.06 – 5.12	A,C
5.13 – 5.19	B,C
5.20 – 5.26	A,B,C

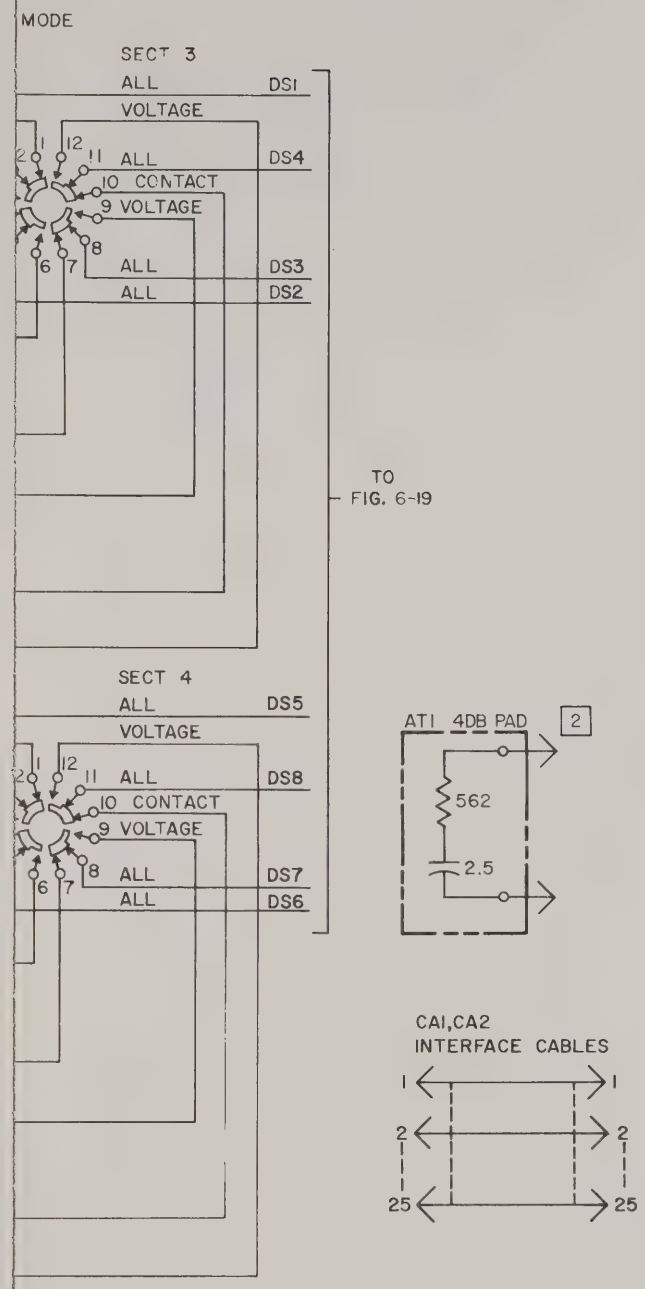
[4] FOR 230 VAC OPERATION REMOVE TRANSFORMER T1 AND INSTALL NEW T1 SIERRA PART NUMBER AND RESISTOR RX, 68K 1/4 WATT SIERRA PART NUMBER 905200683.

VOLTAGE CHART

READINGS WERE TAKEN USING A 20 KΩ/VOLT DC, 5 KΩ/VOLT AC METER.

DEVICE	E	B	C	CATHODE	ANODE	GATE	
CHASSIS Q1	21.0	20.8	11.8	To protect the logic CK Integrated Circuits, remove all leads from CP-13 pins 26 & 27 except the collector lead of chassis-mounted Q3. This is very important if the +5V crowbar circuit is inoperative			
CHASSIS Q2	-11.3	-11.5	-21.8				
CHASSIS Q3	10.9	10.6	4.75				
CP-13 Q1	11.8	12.2	20.8				
CP-13 Q2	4.8	5.6	10.6				
CP-13 Q3				0.0	10.9	0.0	
CP-13 CR1				225	200Vac		Readings taken with fuses F2, F3, F4 pulled.
CP-13 CR2				27	20Vac		
CP-13 CR3				20Vac	-27		
CP-13 CR4				27	20Vac		
CP-13 CR5				20Vac	-27		
CP-13 CR6				12.2	0		
CP-13 CR7				6.9	0		
CP-13 CR8				4.8	0.3		
CP-13 CR9				0	-11.4		
CP-13 CR10				13V	10Vac		Readings taken with F5 pulled.
CP-13 CR11				13V	10Vac		

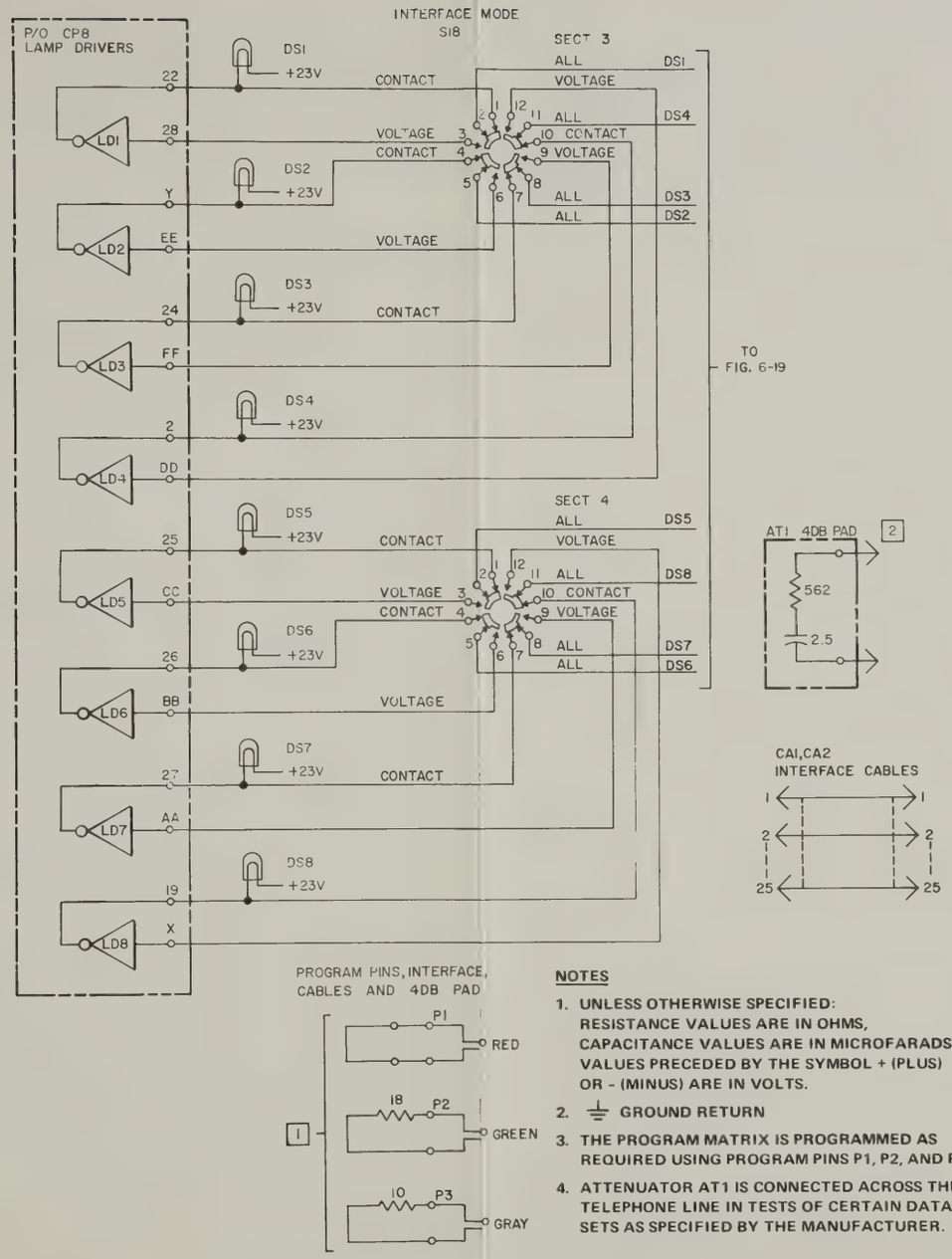
Figure 6-27. Power Supply



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. THE PROGRAM MATRIX IS PROGRAMMED AS REQUIRED USING PROGRAM PINS P1, P2, AND P3.
4. ATTENUATOR AT1 IS CONNECTED ACROSS THE TELEPHONE LINE IN TESTS OF CERTAIN DATA SETS AS SPECIFIED BY THE MANUFACTURER.

Figure 6-28. Lamp Drivers, Program Pins, Interface Cables, and 40 dB pad.



NOTES

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. THE PROGRAM MATRIX IS PROGRAMMED AS REQUIRED USING PROGRAM PINS P1, P2, AND P3.
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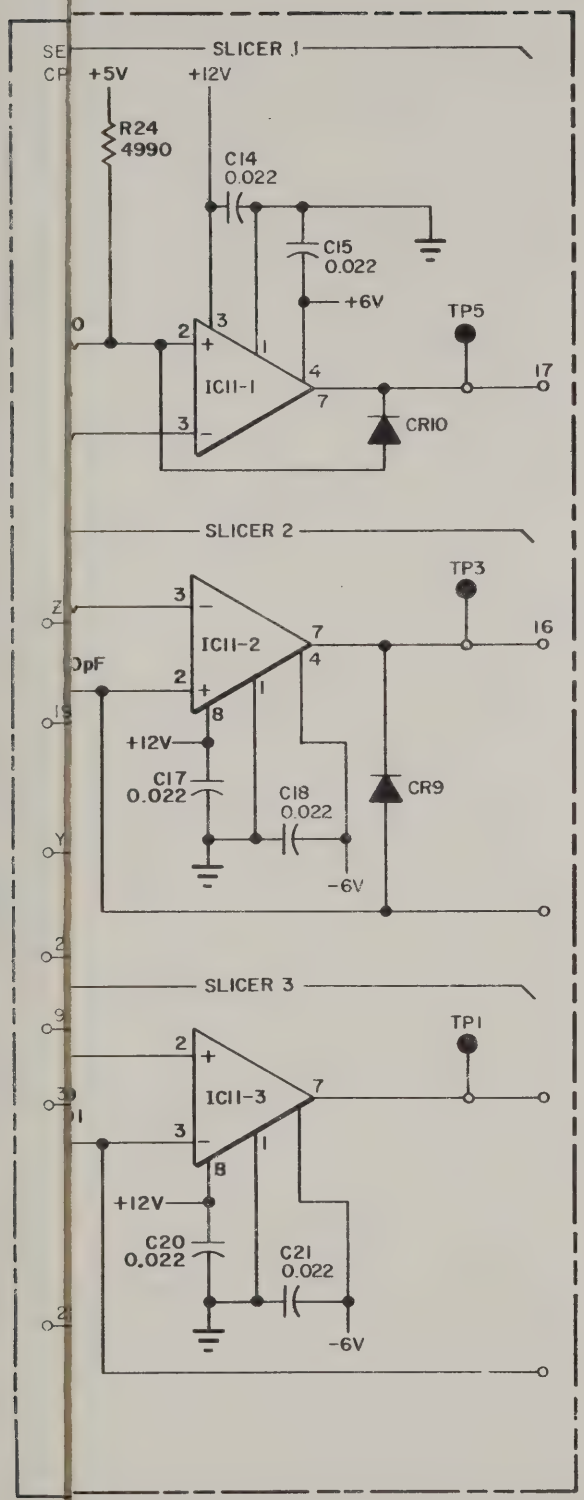
Figure 6-28. Lamp Drivers, Program Pins, Interface Cables, and 40 dB pad.



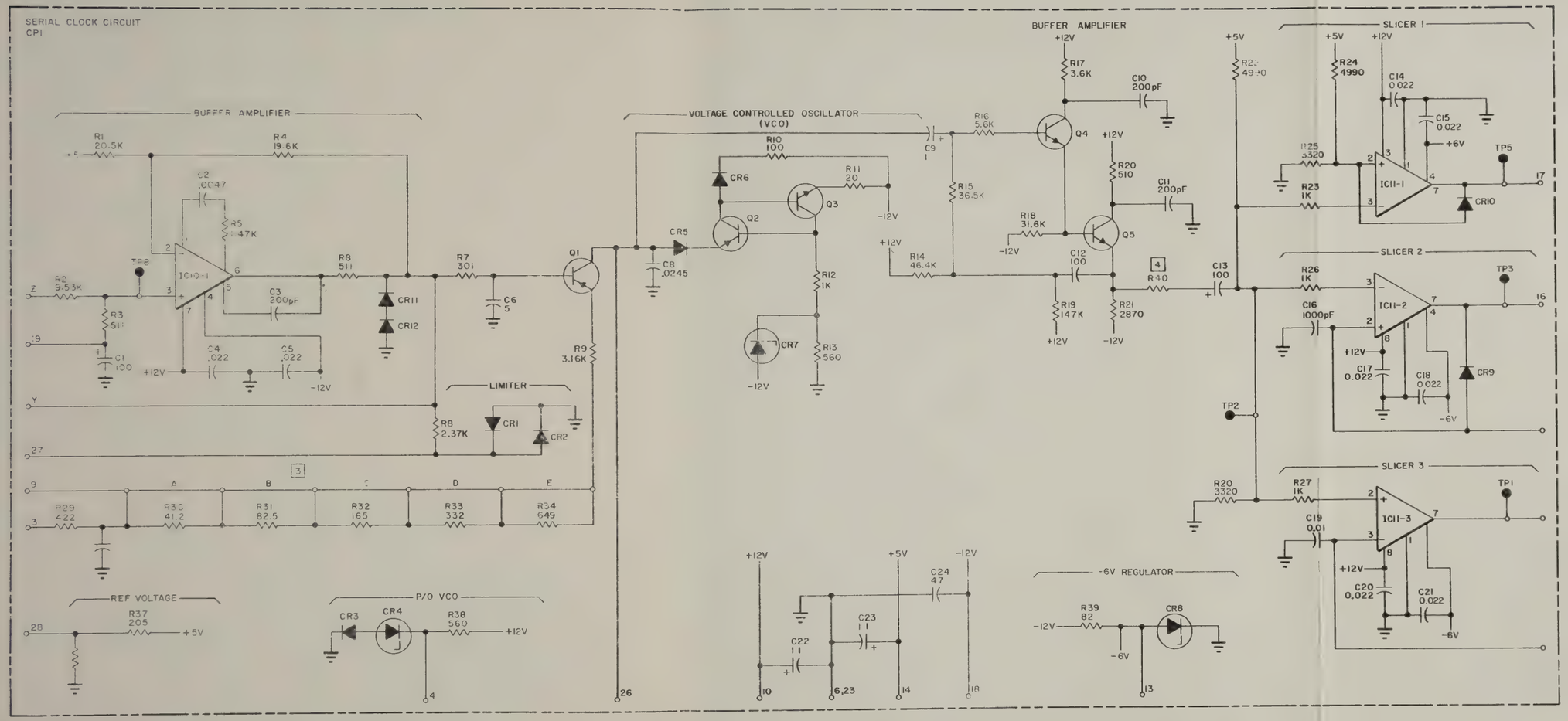
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS.
   CAPACITANCE VALUES ARE IN MICROFARADS.
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. STRAPS A THROUGH E ARE CUT AS REQUIRED TO ESTABLISH PROPER OUTPUT FREQUENCY. IF FREQUENCY IS OUT OF SPEC RE-INSTALL STRAPS A THROUGH E. MEASURE FREQUENCY WITH ALL STRAPS INSTALLED, AND CUT STRAPS AS SHOWN IN TABLE BELOW.

MEASURE FREQUENCY	CUT STRAPS
9945 – 10053	
10054 – 10160	A
10161 – 10267	B
10268 – 10374	A,B
10375 – 10481	C
10482 – 10587	A,C
10588 – 10694	B,C
10695 – 10800	A,B,C
10801 – 10906	D
10907 – 11012	A,D
11013 – 11118	B,D
11119 – 11224	A,B,D
11225 – 11330	C,D
11331 – 11435	A,C,D
11436 – 11540	B,C,D
11541 – 11645	A,B,C,D
11646 – 11751	E
11752 – 11855	A,E
11856 – 11960	B,E
11961 – 12065	A,B,E
12066 – 12169	C,E
12170 – 12274	A,C,E
12275 – 12378	B,C,E
12379 – 12482	A,B,C,E
12483 – 12586	D,E
12587 – 12689	A,D,E
12690 – 12793	B,D,E
12794 – 12896	A,B,D,E
12897 – 13000	C,D,E
13001 – 13103	A,C,D,E
13104 – 13206	B,C,D,E
13207 – 13329	A,B,C,D,E

4. STRAPS A THROUGH E ARE CUT AS REQUIRED DURING MANUFACTURING TESTING.
5. A VALUE OF 301 OHMS SHALL BE INSTALLED DURING CIRCUIT BOARD MANUFACTURE. AT THE TIME OF MANUFACTURING TESTING OF THE ASSEMBLED 1914B THE SAMPLE WINDOW IS CHECKED. IF THE WINDOW WIDTH IS GREATER THAN THAT SPECIFIED IN THE TEST REQUIREMENTS (R40) SHOULD BE CHANGED TO 162 OHMS. IF THE WINDOW IS NOT WIDE ENOUGH (R40) SHOULD BE CHANGED TO 422 OHMS.

Figure 6-29. CP1 Serial Clock Circuit



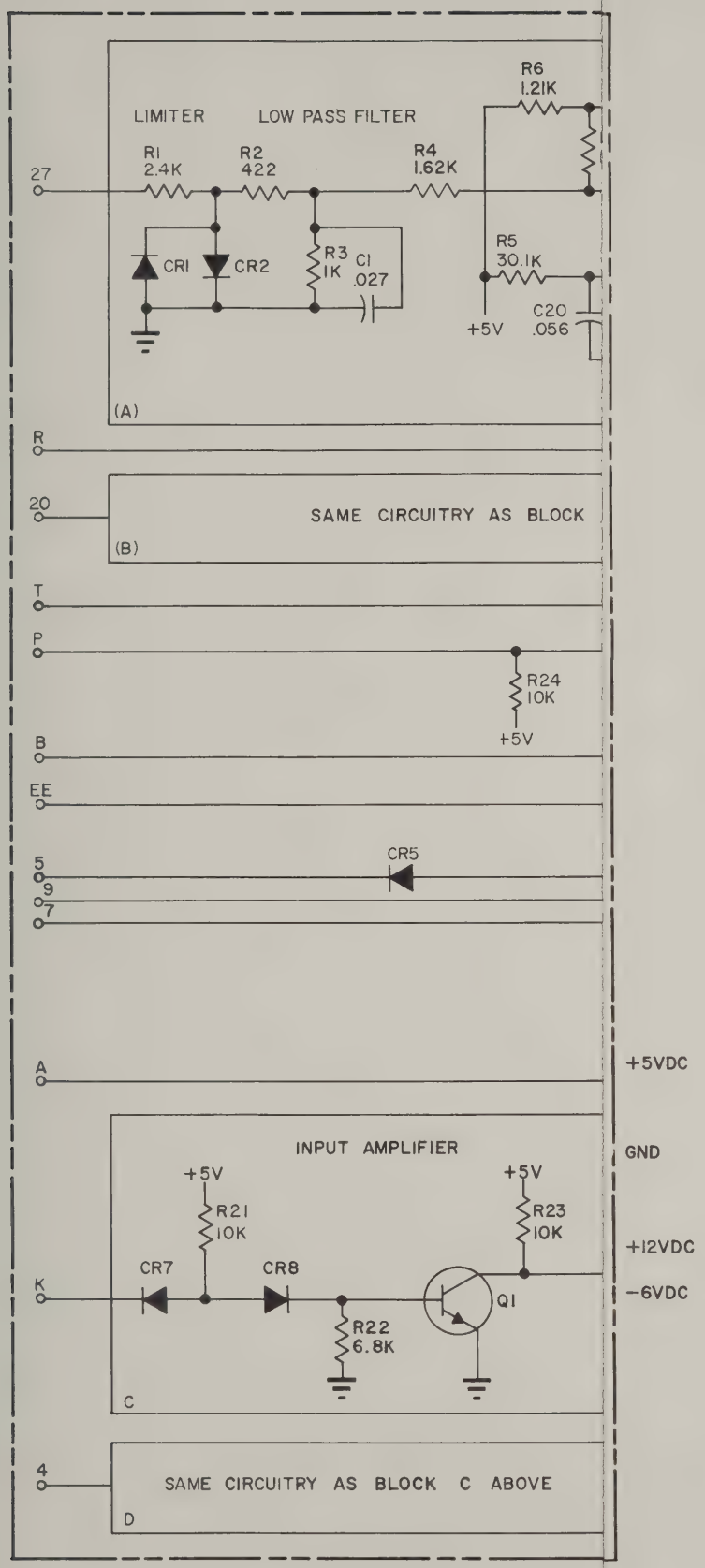
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS.
   CAPACITANCE VALUES ARE IN MICROFARADS.
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. STRAPS A THROUGH E ARE CUT AS REQUIRED TO ESTABLISH PROPER OUTPUT FREQUENCY. IF FREQUENCY IS OUT OF SPEC RE-INSTALL STRAPS A THROUGH E. MEASURE FREQUENCY WITH ALL STRAPS INSTALLED, AND CUT STRAPS AS SHOWN IN TABLE BELOW.

MEASURE FREQUENCY	CUT STRAPS
9945 – 10053	
10054 – 10160	A
10161 – 10267	B
10268 – 10374	A,B
10375 – 10481	C
10482 – 10587	A,C
10588 – 10694	B,C
10695 – 10800	A,B,C
10801 – 10906	D
10907 – 11012	A,D
11013 – 11118	B,D
11119 – 11224	A,B,D
11225 – 11330	C,D
11331 – 11435	A,C,D
11436 – 11540	B,C,D
11541 – 11645	A,B,C,D
11646 – 11751	E
11752 – 11855	A,E
11856 – 11960	B,E
11961 – 12065	A,B,E
12066 – 12169	C,E
12170 – 12274	A,C,E
12275 – 12378	B,C,E
12379 – 12482	A,B,C,E
12483 – 12586	D,E
12587 – 12689	A,D,E
12690 – 12793	B,D,E
12794 – 12896	A,B,D,E
12897 – 13000	C,D,E
13001 – 13103	A,C,D,E
13104 – 13206	B,C,D,E
13207 – 13329	A,B,C,D,E

4. STRAPS A THROUGH E ARE CUT AS REQUIRED DURING MANUFACTURING TESTING.
5. A VALUE OF 301 OHMS SHALL BE INSTALLED DURING CIRCUIT BOARD MANUFACTURE. AT THE TIME OF MANUFACTURING TESTING OF THE ASSEMBLED 1914B THE SAMPLE WINDOW IS CHECKED. IF THE WINDOW WIDTH IS GREATER THAN THAT SPECIFIED IN THE TEST REQUIREMENTS (R40) SHOULD BE CHANGED TO 162 OHMS. IF THE WINDOW IS NOT WIDE ENOUGH (R40) SHOULD BE CHANGED TO 422 OHMS.

Figure 6-29. CP1 Serial Clock Circuit

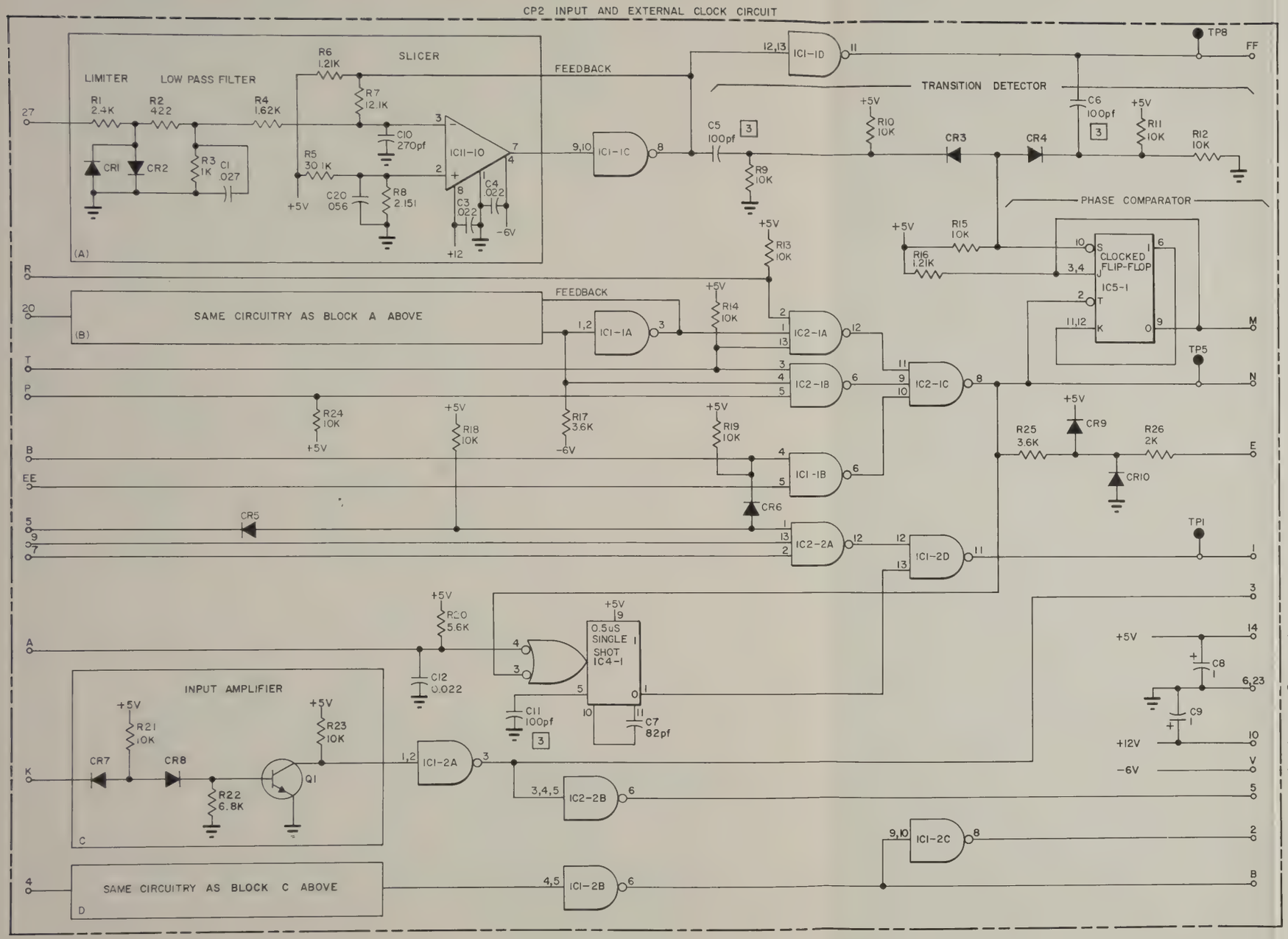


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. SOME EARLY PRODUCTION UNITS ARE EQUIPPED WITH 110 pF CAPACITORS (CODE CD6FC111J603).
4. VOLTAGE AND GROUND TERMINALS FOR IC'S:

IC	+5V	GRD
IC1 - IC5	14	7

Figure 6-30. CP2 Input and External Clock Circuit

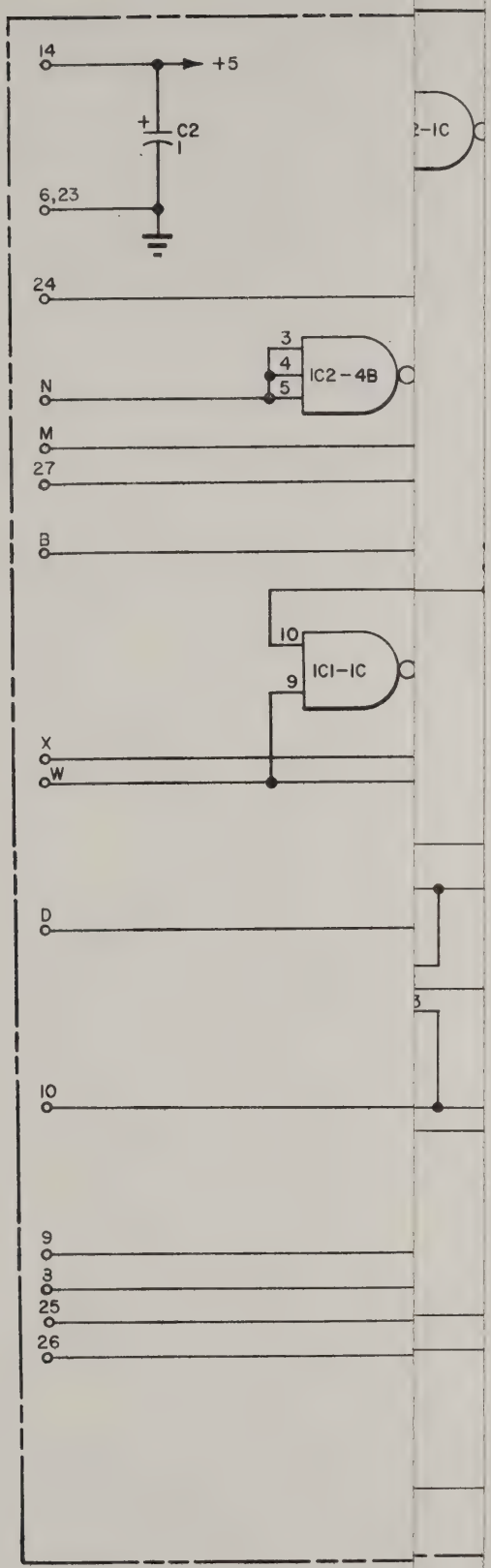


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. SOME EARLY PRODUCTION UNITS ARE EQUIPPED WITH 110 pF CAPACITORS (CODE CD6FC111J603).
4. VOLTAGE AND GROUND TERMINALS FOR IC'S:

IC	+5V	GRD
IC1 - IC5	14	7

Figure 6-30. CP2 Input and External Clock Circuit

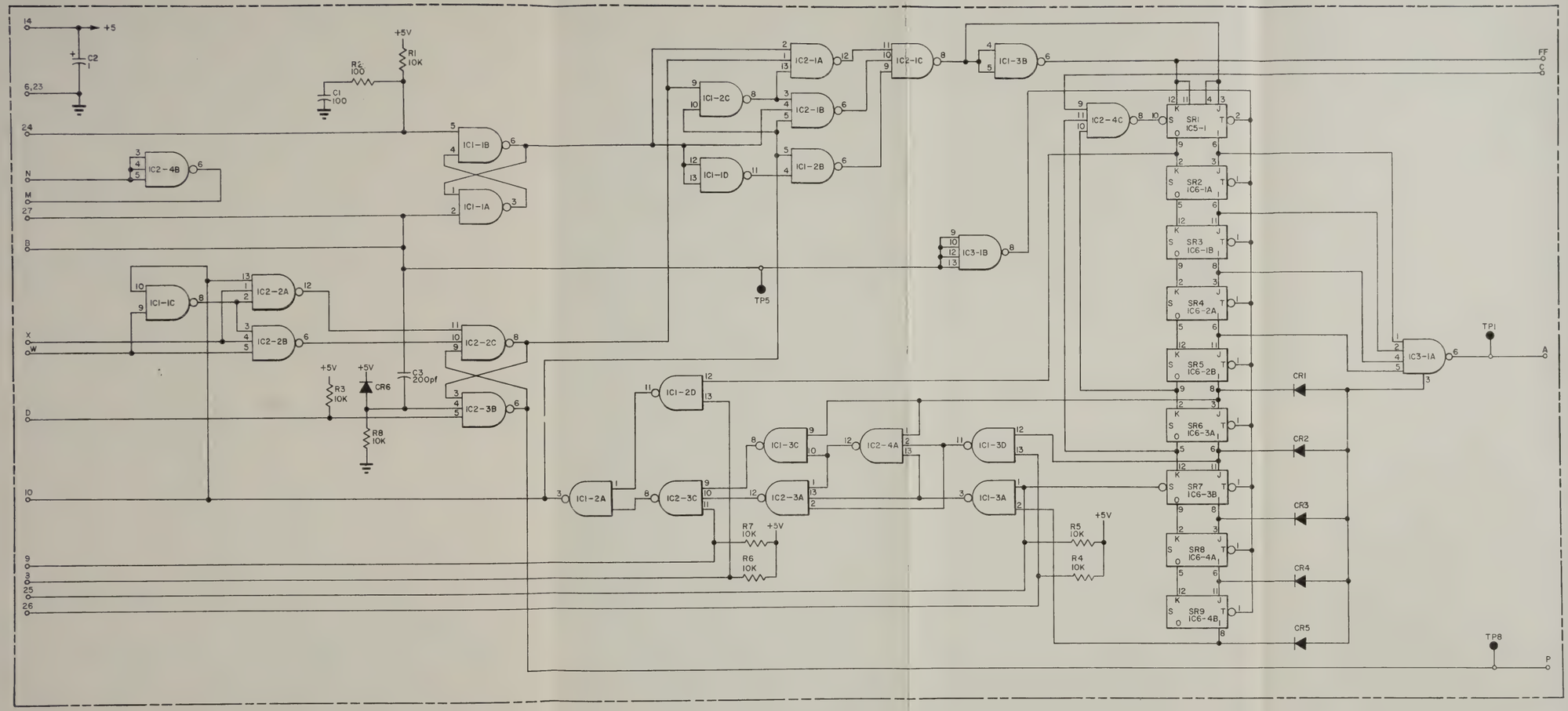


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL +(PLUS) or -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. VOLTAGES AND GROUND TERMINALS FOR IC's:

IC	+5V	GRD
IC1 - IC6	14	7

Figure 6-31. CP3 Word Generator Circuit

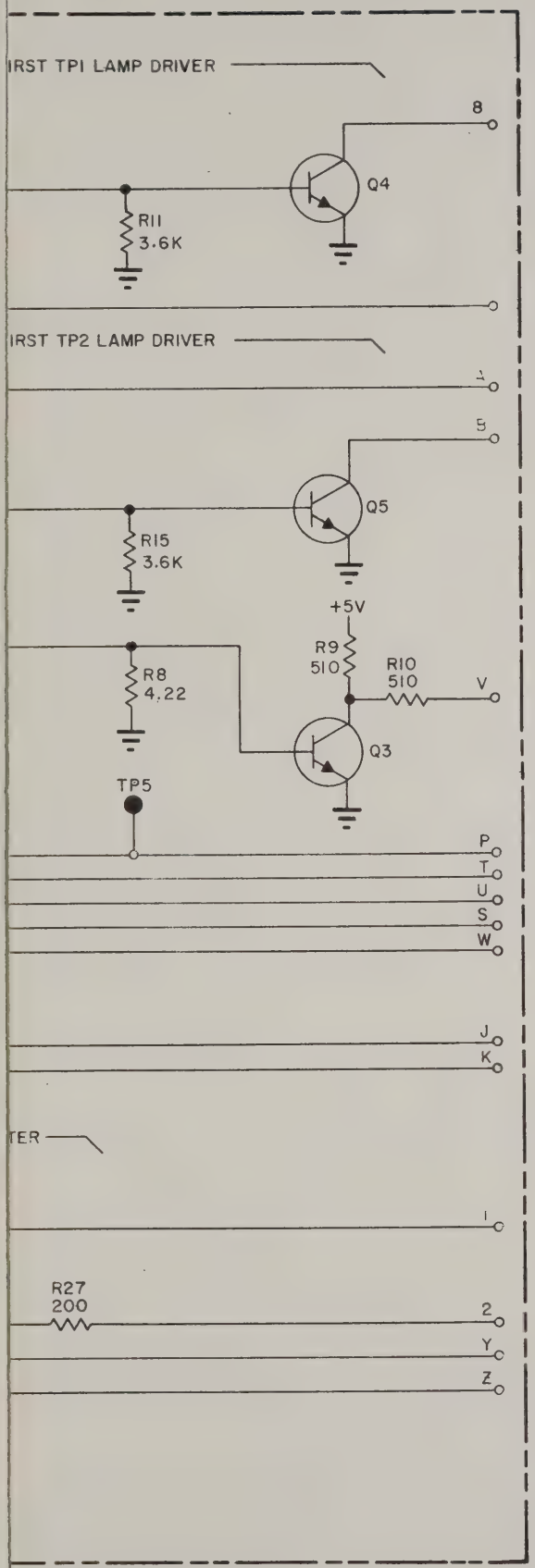


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL +(PLUS) or -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. VOLTAGES AND GROUND TERMINALS FOR IC's:

IC	+5V	GRD
IC1 - IC6	14	7

Figure 6-31. CP3 Word Generator Circuit

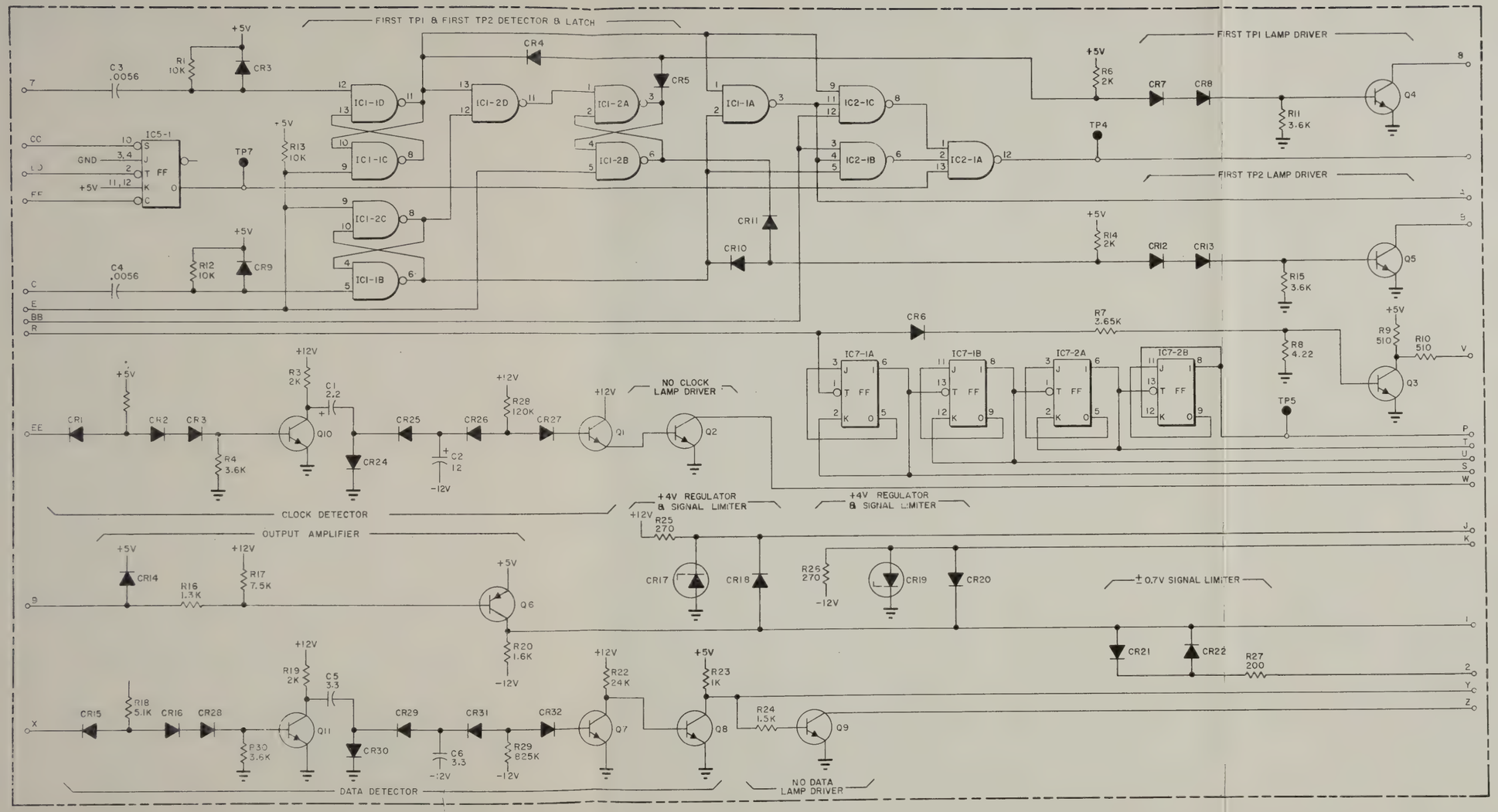


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. VOLTAGE AND GROUND TERMINALS FOR IC'S

IC	+5	GRD
IC-	14	7

Figure 6-32. CP4 Output Amplifier, Detector, and Block Counter Circuit

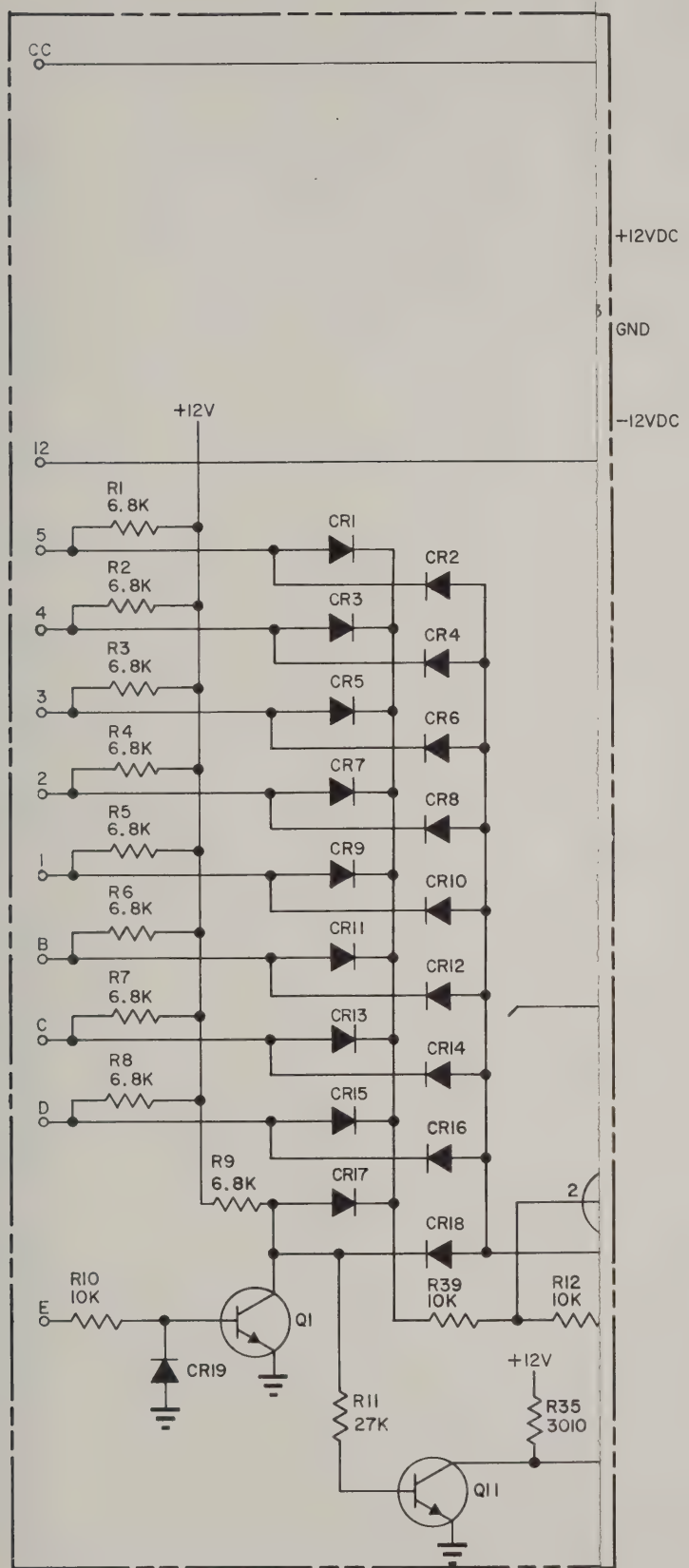


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. VOLTAGE AND GROUND TERMINALS FOR IC'S

IC	+5	GRD
IC-	14	7

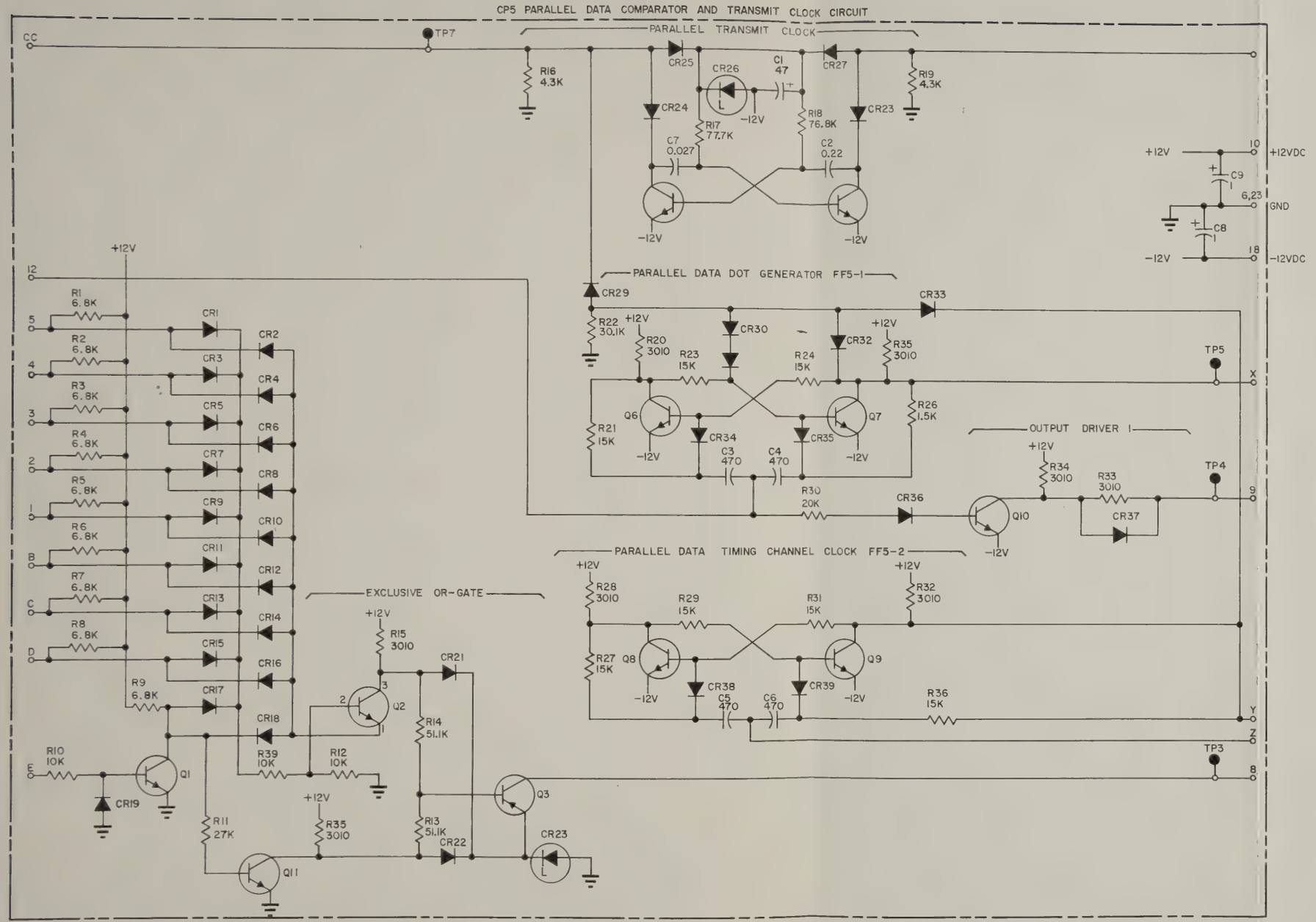
Figure 6-32. CP4 Output Amplifier, Detector, and Block Counter Circuit



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.

Figure 6-33. CP5 Parallel Data Comparator and Transmit Clock Circuit



NOTES:

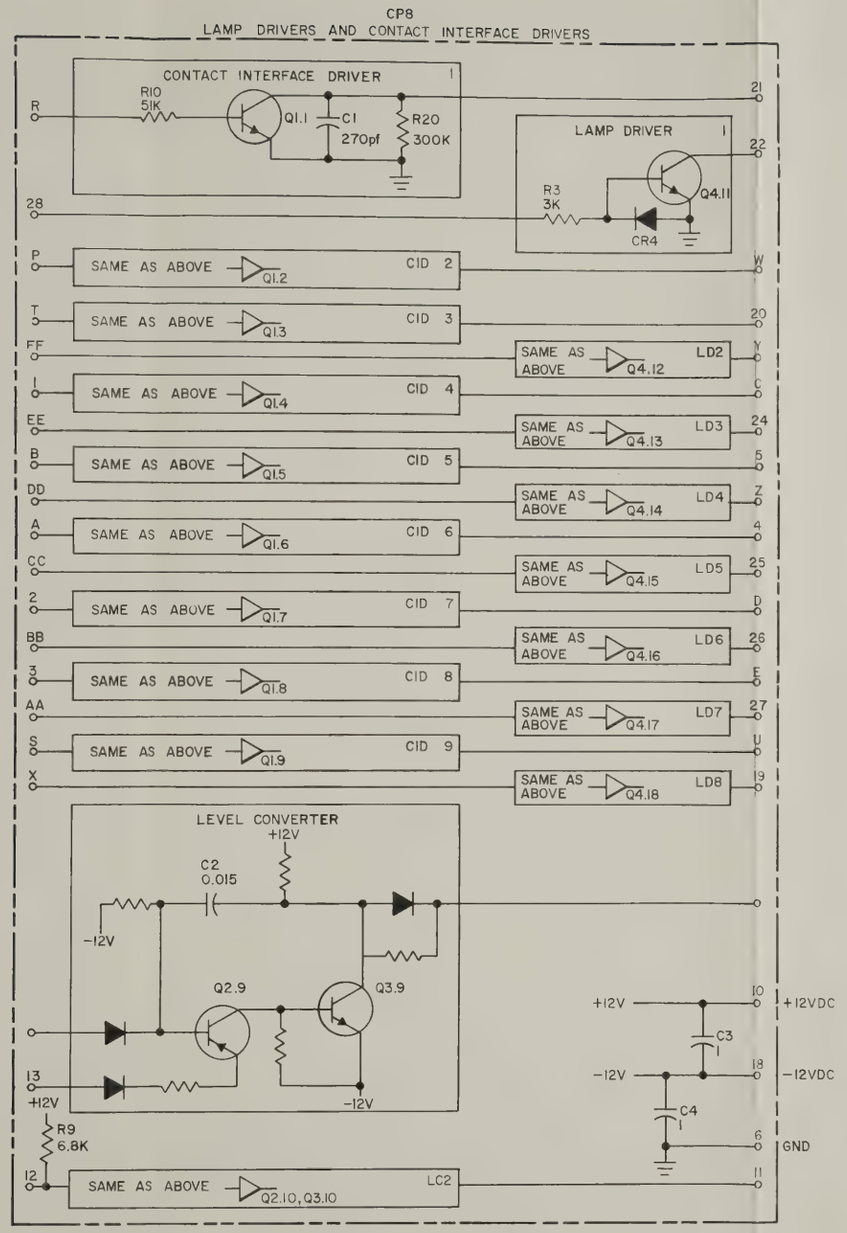
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.

Figure 6-33. CP5 Parallel Data Comparator and Transmit Clock Circuit

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS; CAPACITANCE VALUES ARE IN MICROFARADS; VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.

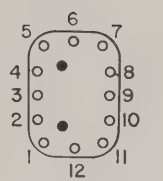
Figure 6-34. CP8 Lamp Drivers and Contact Interface Drivers



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS; CAPACITANCE VALUES ARE IN MICROFARADS; VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.

Figure 6-34. CP8 Lamp Drivers and Contact Interface Drivers



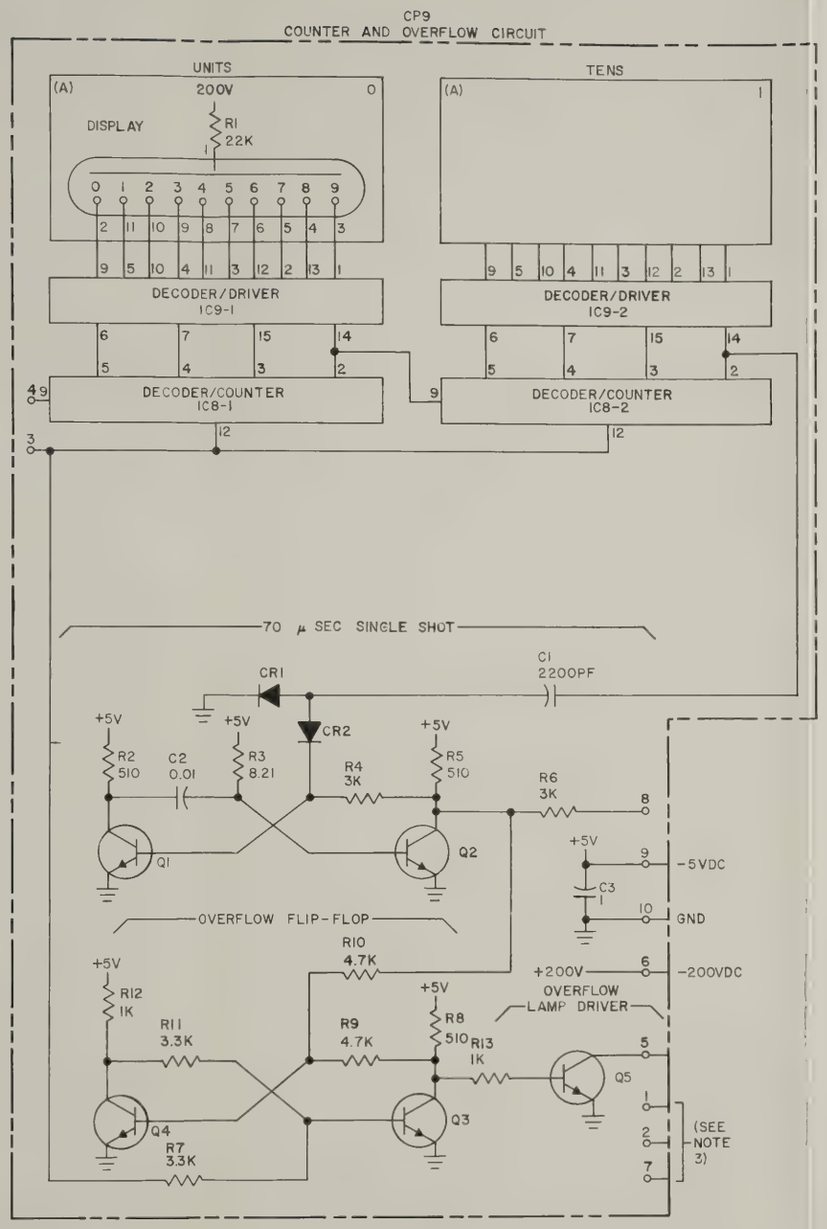
NIXIE TUBE
BOTTOM VIEW

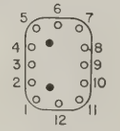
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. TERMINALS 1, 2 AND 7 ARE USED AS TIE POINTS
4. VOLTAGE AND GROUND TERMINALS FOR IC'S:

IC	+5	GRD
IC8	14	7
IC9	16	8

Figure 6-35. CP9 Counter and Overflow Circuit





NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. TERMINALS 1, 2 AND 7 ARE USED AS TIE POINTS
4. VOLTAGE AND GROUND TERMINALS FOR IC'S:

IC	+5	GRD
IC8	14	7
IC9	16	8

Figure 6-35. CP9 Counter and Overflow Circuit

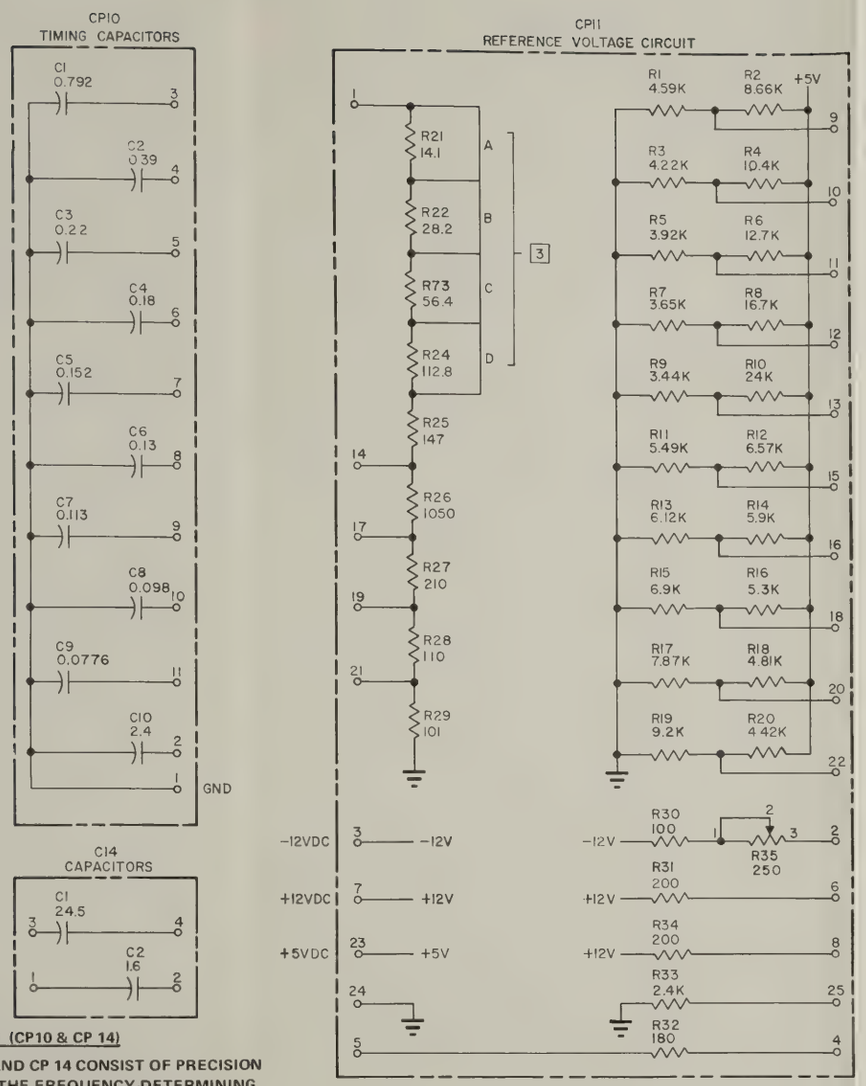
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. STRAPS A THROUGH D ARE CUT AS REQUIRED TO SET THE +7V REFERENCE TO 7.00 ±0.04V.
   THE PROCEDURE IS AS FOLLOWS:
   SET SELECT SWITCH TO +7
   OUTPUT SWITCH TO TP3
   INSTALL SHORTING PIN IN GRD ROW, COL. 1 OF MATRIX.
   CONNECT A 0.1% DIGITAL VOLTMETER FROM TP3 TO INTERFACE SELECTOR SWITCH 1.
   IF THE READING IS NOT 7.00 ±0.04 VDC, INSTALL STRAPS ACROSS ALL POINTS, A THROUGH D.
   REMEASURE AND CUT STRAPS AS INDICATED IN THE FOLLOWING TABLE.

MEASURED VOLTAGE		
GREATER THAN	BUT LESS THAN OR EQUAL TO	CUT STRAPS
6.96	7.04	None
7.04	7.09	A
7.09	7.15	B
7.15	7.21	A,B,
7.21	7.27	C
7.27	7.34	A,C
7.34	7.40	B,C
7.40	7.46	A,B,C
7.46	7.52	D
7.52	7.58	A,D
7.58	7.64	B,D
7.64	7.70	A,B,D
7.70	7.76	C,D
7.76	7.82	A,C,D
7.82	7.88	B,C,D
7.88	7.95	A,B,C,D

IF VOLTAGE IS BELOW 6.96 VOLTS, CHECK CR1 ON SELECT SWITCH S9.

Figure 6-36. CP10 Timing Capacitors, CP11 Reference Voltage Circuits, and CP14 Capacitors



CIRCUIT DESCRIPTION (CP10 & CP 14)

CIRCUIT PACKS CP10 AND CP 14 CONSIST OF PRECISION CAPACITORS USED IN THE FREQUENCY-DETERMINING PORTION OF THE OSCILLATOR FOUND ON CP1.

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. STRAPS A THROUGH D ARE CUT AS REQUIRED TO SET THE +7V REFERENCE TO 7.00 ±0.04V. THE PROCEDURE IS AS FOLLOWS:
   SET SELECT SWITCH TO +7
   OUTPUT SWITCH TO TP3
   INSTALL SHORTING PIN IN GRD ROW, COL. 1 OF MATRIX.
   CONNECT A 0.1% DIGITAL VOLTMETER FROM TP3 TO INTERFACE SELECTOR SWITCH 1.
   IF THE READING IS NOT 7.00 ±0.04 VDC, INSTALL STRAPS ACROSS ALL POINTS, A THROUGH D.
   REMEASURE AND CUT STRAPS AS INDICATED IN THE FOLLOWING TABLE.

MEASURED VOLTAGE

GREATER THAN	BUT LESS THAN OR EQUAL TO	CUT STRAPS
6.96	7.04	None
7.04	7.09	A
7.09	7.15	B
7.15	7.21	A,B,
7.21	7.27	C
7.27	7.34	A,C
7.34	7.40	B,C
7.40	7.46	A,B,C
7.46	7.52	D
7.52	7.58	A,D
7.58	7.64	B,D
7.64	7.70	A,B,D
7.70	7.76	C,D
7.76	7.82	A,C,D
7.82	7.88	B,C,D
7.88	7.95	A,B,C,D

IF VOLTAGE IS BELOW 6.96 VOLTS, CHECK CR1 ON SELECT SWITCH S9.

Figure 6-36. CP10 Timing Capacitors, CP11 Reference Voltage Circuits, and CP14 Capacitors

−12V

+12V

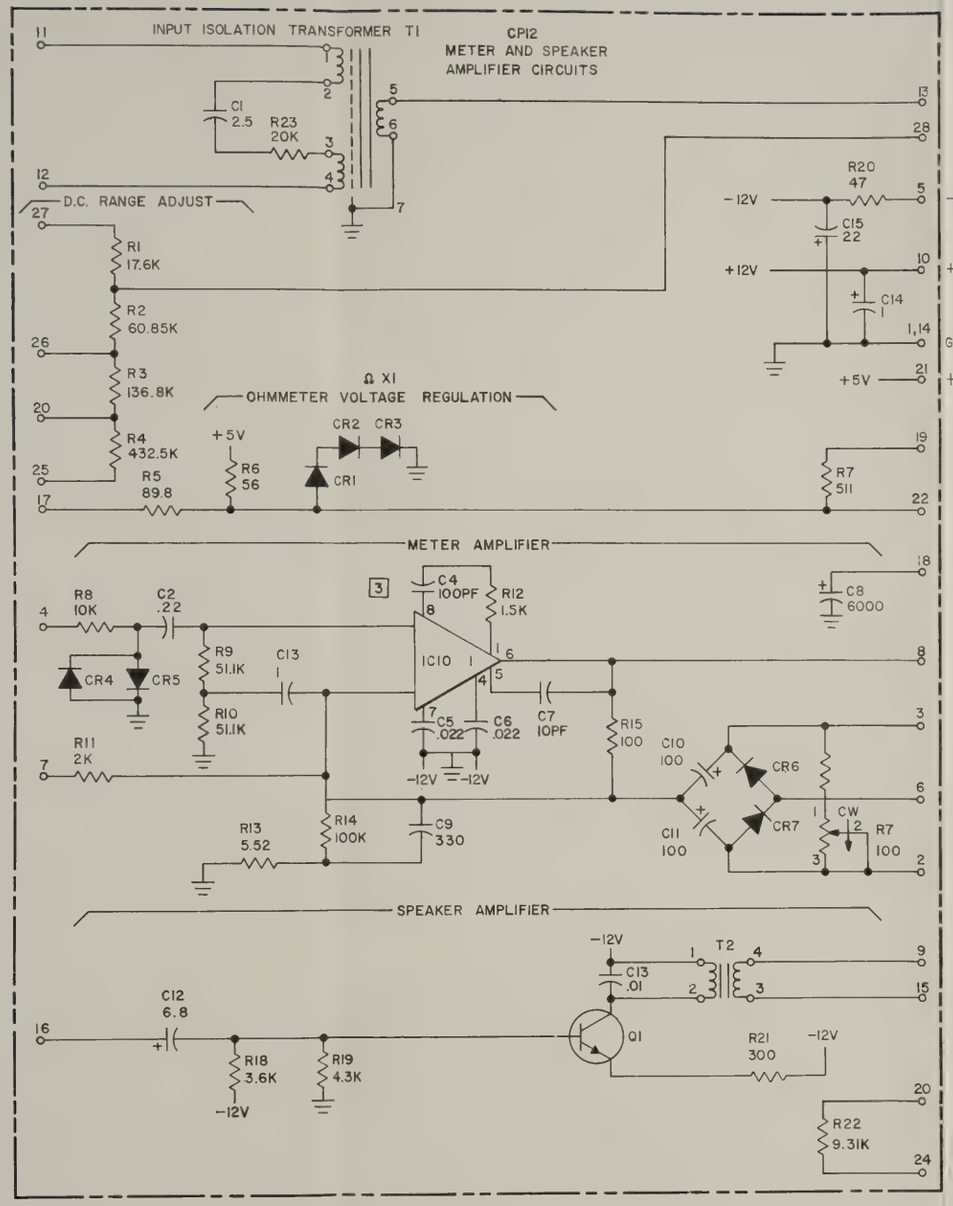
GND

+5VDC

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. SOME EARLY PRODUCTION UNITS ARE EQUIPPED WITH 110pF CAPACITORS (CODE CD-6FC111103).

Figure 6-37. CP12 Meter and Speaker Amplifier Circuit



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN
3. SOME EARLY PRODUCTION UNITS ARE EQUIPPED WITH 110pF CAPACITORS (CODE CD-6FC111103).

Figure 6-37. CP12 Meter and Speaker Amplifier Circuit

IC1-A (A)

CODE

U6A994659X, FAIRCHILD OR PD9946

CIRCUIT DESCRIPTION

THIS ICM CONTAINS 4 POSITIVE LOG CONSISTING
NAND GATES. THE LOGIC FUNCTIO WORK TO
X_1 AND X_2 IS SHOWN IN THE TRUTH THE CIRCUIT
IVE TRANSITION

INPUT		OUTP
X_1	X_2	F
0	0	1
0	1	1
1	0	1
1	1	0

IC2- (B)

CODE

U6A996259X, FAIRCHILD OR PD9962

CIRCUIT DESCRIPTION

THIS ICM CONTAINS 3 3-INPUT POSI
NAND GATES.

IC3- (C)

CODE

U6A993259X, FAIRCHILD OR PD-993

CIRCUIT DESCRIPTION

THIS ICM COMPRISES 2 4-INPUT EXP
TIVE LOGIC DTL NAND GATES WITH S 6, 7, 15,
CAPABILITY. PINS 3 AND 11 ARE TH UTPUT ON
INPUTS. ABLE FOR

IC4- (D)

CODE

U6A . . 159X, FAIRCHILD

CIRCUIT DESCRIPTION

THIS ICM CONSISTS OF A MONOSTAB
VIBRATOR THAT TRIGGERS IN RESP
NEGATIVE TRANSITIONS OF THE SI
PLIED TO PINS 3 AND 4. THE PULSE
IS DETERMINED BY THE VALUE OF
NAL CAPACITOR CONNECTED BETW
AND 11 AND THE INTERNAL TIMING
(PINS 9-10). AN EXTERNAL CAPACIT
CONNECTED FROM PIN 5 TO GROUN
THE NOISE SENSITIVITY OF THE CI

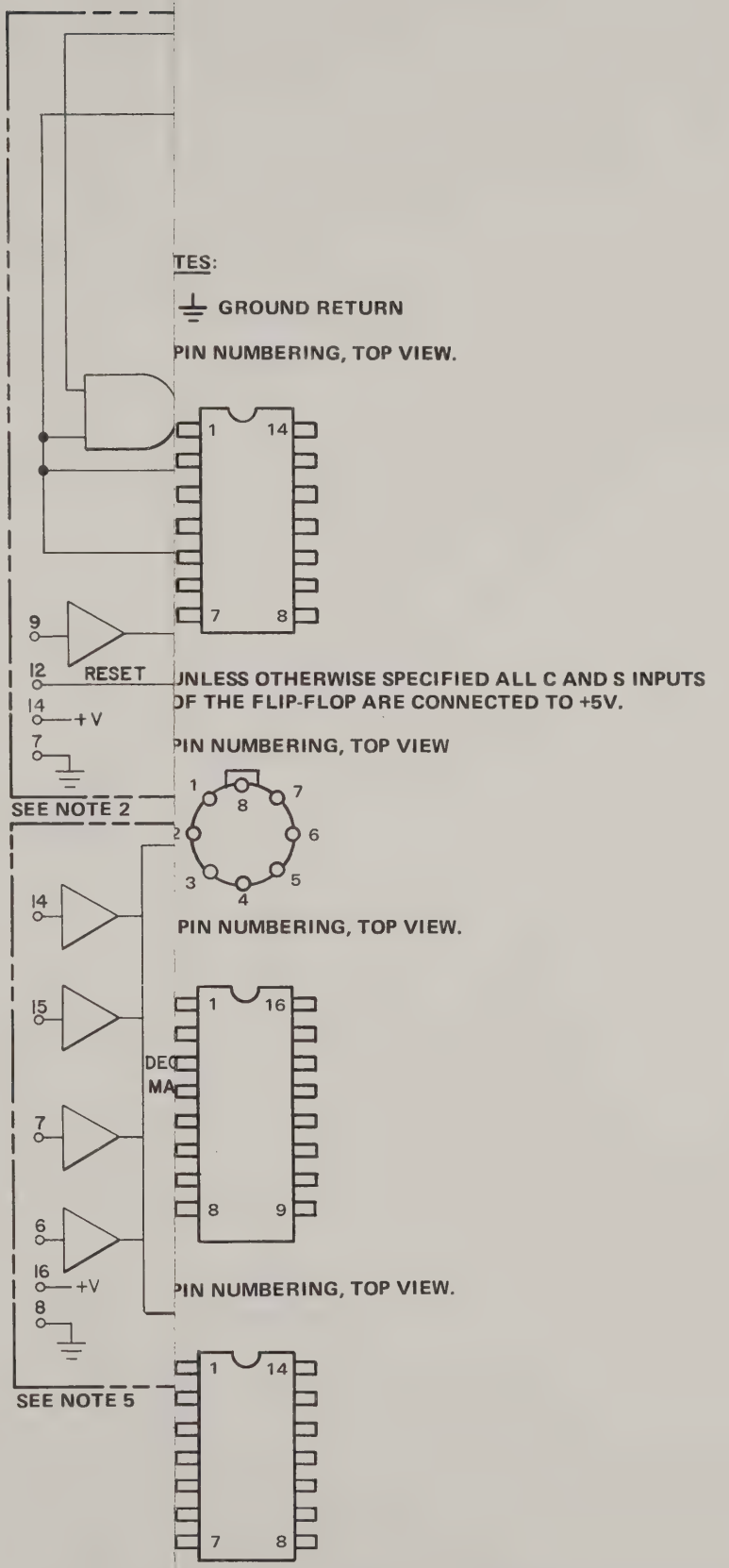


Figure 6-38. Integrated Circuit Modules

IC1-A (A)

CODE

U6A994659X, FAIRCHILD OR PD9946-59, PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM CONTAINS 4 POSITIVE LOGIC DTL 2-INPUT NAND GATES. THE LOGIC FUNCTION FOR 2 INPUTS, X_1 AND X_2 IS SHOWN IN THE TRUTH TABLE BELOW:

INPUT		OUTPUT
X_1	X_2	F
0	0	1
0	1	1
1	0	1
1	1	0

IC2- (B)

CODE

U6A996259X, FAIRCHILD OR PD9962-59, PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM CONTAINS 3 3-INPUT POSITIVE LOGIC DTL NAND GATES.

IC3- (C)

CODE

U6A993259X, FAIRCHILD OR PD-9932-59, PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM COMPRISES 2 4-INPUT EXPANDABLE, POSITIVE LOGIC DTL NAND GATES WITH HIGH FAN-OUT CAPABILITY. PINS 3 AND 11 ARE THE EXPANDER INPUTS.

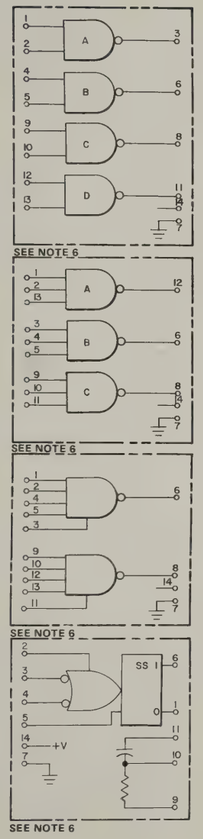
IC4- (D)

CODE

U6A . . 159X, FAIRCHILD

CIRCUIT DESCRIPTION

THIS ICM CONSISTS OF A MONOSTABLE MULTIVIBRATOR THAT TRIGGERS IN RESPONSE TO NEGATIVE TRANSITIONS OF THE SIGNALS APPLIED TO PINS 3 AND 4. THE PULSE DURATION IS DETERMINED BY THE VALUE OF THE EXTERNAL CAPACITOR CONNECTED BETWEEN PINS 10 AND 11 AND THE INTERNAL TIMING RESISTOR (PINS 9-10). AN EXTERNAL CAPACITOR MAY BE CONNECTED FROM PIN 5 TO GROUND TO REDUCE THE NOISE SENSITIVITY OF THE CIRCUIT.



IC5- (E)

CODE

U6A994559X, FAIRCHILD OR PD9945-59, PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM CONSISTS OF A CLOCKED FLIP-FLOP WITH DIRECT SET (S; PIN 10) AND CLEAR (C; PIN 5) INPUTS. THE LOGIC STATE PRESENT ON THE J AND K LEADS IS INSERTED INTO THE FLIP-FLOP WHEN THE T LEAD (P1 I 2) CHANGES FROM A 1 TO A 0.

IC6- (F)

CODE

U6A909459X, FAIRCHILD OR PD9094-59 PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM COMPRISES TWO CLOCKED FLIP-FLOPS WITH SEPARATE SET INPUTS (PINS 4 AND 10) AND COMMON CLEAR (PIN 13) AND TOGGLE (T; PIN 1) INPUTS. THE SIGNAL PRESENT ON THE J-K LEADS (PINS 3, 2 AND 11, 12) IS SHIFTED INTO THE FLIP-FLOP IN RESPONSE TO A NEGATIVE TRANSITION OF THE SIGNAL ON T INPUT.

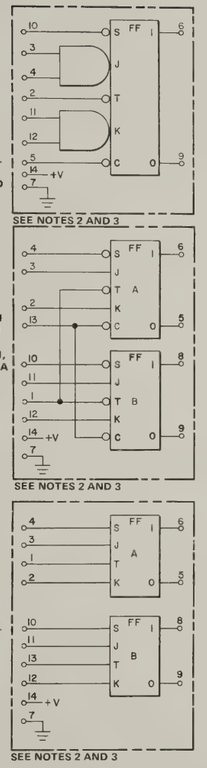
IC7- (G)

CODE

U6A909759X, FAIRCHILD OR PD9097-59, PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM CONTAINS 2 CLOCKED FLIP-FLOPS OF THE IC5 TYPE. INDEPENDENT SET (S), J AND K, AND TOGGLE (T) INPUTS ARE PROVIDED FOR EACH FLIP-FLOP.



IC8- (H)

CODE

U6A995879X, FAIRCHILD

CIRCUIT DESCRIPTION

THIS ICM CONTAINS A DECADE COUNTER CONSISTING OF 4 FLIP-FLOPS WITH A FEEDBACK NETWORK TO PROVIDE A BCD OUTPUT (PINS 5, 4, 3, 2). THE CIRCUIT REGISTERS A COUNT FOR EVERY NEGATIVE TRANSITION OF THE INPUT SIGNAL (PIN 9).

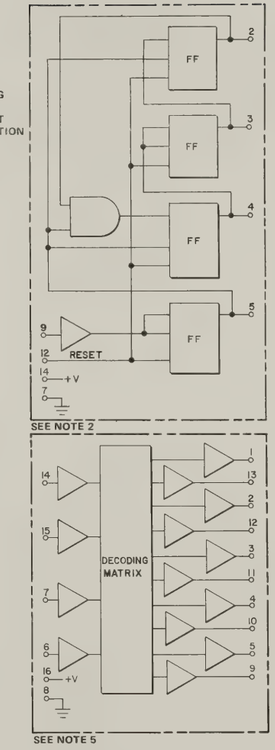
IC9- (I)

CODE

U6B96079X, FAIRCHILD

CIRCUIT DESCRIPTION

THIS ICM ACCEPTS A BCD INPUT ON LEADS 6, 7, 15, AND 14 AND PROVIDES A 0 VOLTAGE OUTPUT ON ONE OF 10 LEADS. THE OUTPUT IS SUITABLE FOR DRIVING NIXIE DISPLAY TUBES.



IC10- (J)

CODE

U5B770939X, FAIRCHILD OR PA7709-39 PHILCO-FORD

CIRCUIT DESCRIPTION

THIS ICM CONTAINS A HIGH-GAIN DC AMPLIFIER WITH A DIFFERENTIAL INPUT (PINS 3 AND 2) AND A SINGLE-ENDED OUTPUT (PIN 6). PIN 1 AND 8 AND PIN 5 ARE FOR EXTERNAL CONNECTIONS OF HIGH-FREQUENCY COMPENSATION NETWORKS.

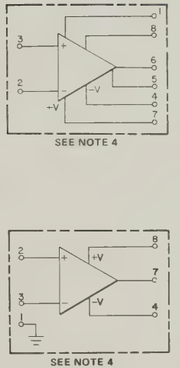
IC11- (K)

CODE

U5B771039X, FAIRCHILD OR PA7710-39 PHILCO-FORD

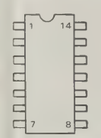
CIRCUIT DESCRIPTION

THIS ICM COMPRISES A HIGH-SPEED, HIGH-GAIN, DIFFERENTIAL COMPARATOR. THE INPUTS ARE PINS 2 AND 3 AND THE OUTPUT IS ON PIN 7.



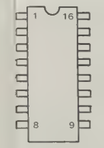
NOTES:

1. ⏚ GROUND RETURN
2. PIN NUMBERING, TOP VIEW.



3. UNLESS OTHERWISE SPECIFIED ALL C AND S INPUTS OF THE FLIP-FLOP ARE CONNECTED TO +5V.
4. PIN NUMBERING, TOP VIEW

5. PIN NUMBERING, TOP VIEW.



6. PIN NUMBERING, TOP VIEW.

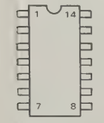


Figure 6-38. Integrated Circuit Modules

SECTION 7
MAINTENANCE

7.01 Maintenance as outlined in this section is divided into two categories. One category deals with the testing and/or calibration of individual circuit groups of the test set, and the other deals with overall operational testing between two test sets, one operating under the transmit mode and the other under the receive mode of operation. For the latter category separate tests are provided for serial and parallel operation. It is strongly recommended that these latter two tests be performed at least once a year.

7.02 The testing and/or calibration procedures of individual circuit groups included under separate paragraph headings are as follows: fuses, control signals, interval counter, word generator and clock, parallel data circuits, reference voltages, clock circuits, data and sample circuits, and the AC voltmeter circuit. Test equipment is required for a few of the tests and is listed in Table 7-1.

7.03 In the event that corrective maintenance of circuits is required, conventional troubleshooting and repair techniques may be used providing that the customary precautions concerning semiconductor devices and printed-circuit boards are observed. A list of replaceable parts is provided in Section 8.

7.04 For access to the internal parts and to various test points on the CP boards, take off the test-set cover (turning power off first to prevent shorting Q1 and Q3 to case), loosen the four quick-release fasteners at the back of the test-set case, and (with the front panel facing up) lift the test-set assembly out of its case. If necessary, CP1 through CP5 and CP8 may be readily removed by loosening the board-retainer screws, sliding the retainer clear of the CP-board edges, and unplugging the CP(s). For dynamic troubleshooting, an extender card may be used with these CP's allowing operation and test with the CP extended from the CP-rack assembly. Other CP's and certain independently mounted parts of the power supply (C1-C3 and Q1-Q3) are "hard-wired" into the test set.

CAUTION: To ensure testing capability and to prevent damage to components, make sure that all test leads and matrix pins have been removed, that all interface selector switches are depressed, and that all interface connecting cables are free of shorts, opens, and crosses before proceeding with any test in this section.

Replacement Fuses, Lamps, Lenses, Shorting Pins, Plug-In Boards (CP's) and Test Points

7.05 If any fuses or lamps are to be replaced as the result of the tests, select replacements according to the following tabulation. Figure 7-3 shows the method of replacing lamps.

WARNING: Use only fuse types specified. Serious damage to the equipment may be caused by improper substitution.

FUSES	REPLACEMENT PARTS
F1	1/2 amp Type MDL Bussman
F2	0.6 amp Type AGC Bussman
F3	1/2 amp Type AGC Bussman
F4	3/8 amp Type AGC Bussman
F5	3/4 amp Type AGC Bussman

Table 7-1. Required Test Equipment

TEST	PARAGRAPH	EQUIPMENT
Clock Circuits	7.13	Frequency Counter: HP 5245L or equivalent
Data and Sample Circuits	7.14	Oscilloscope: Tektronics 543B with dual trace plug-in or equivalent.
AC Voltmeter	7.15	External 600-ohm reference source of 0 dBm accurate within ±0.1 dB

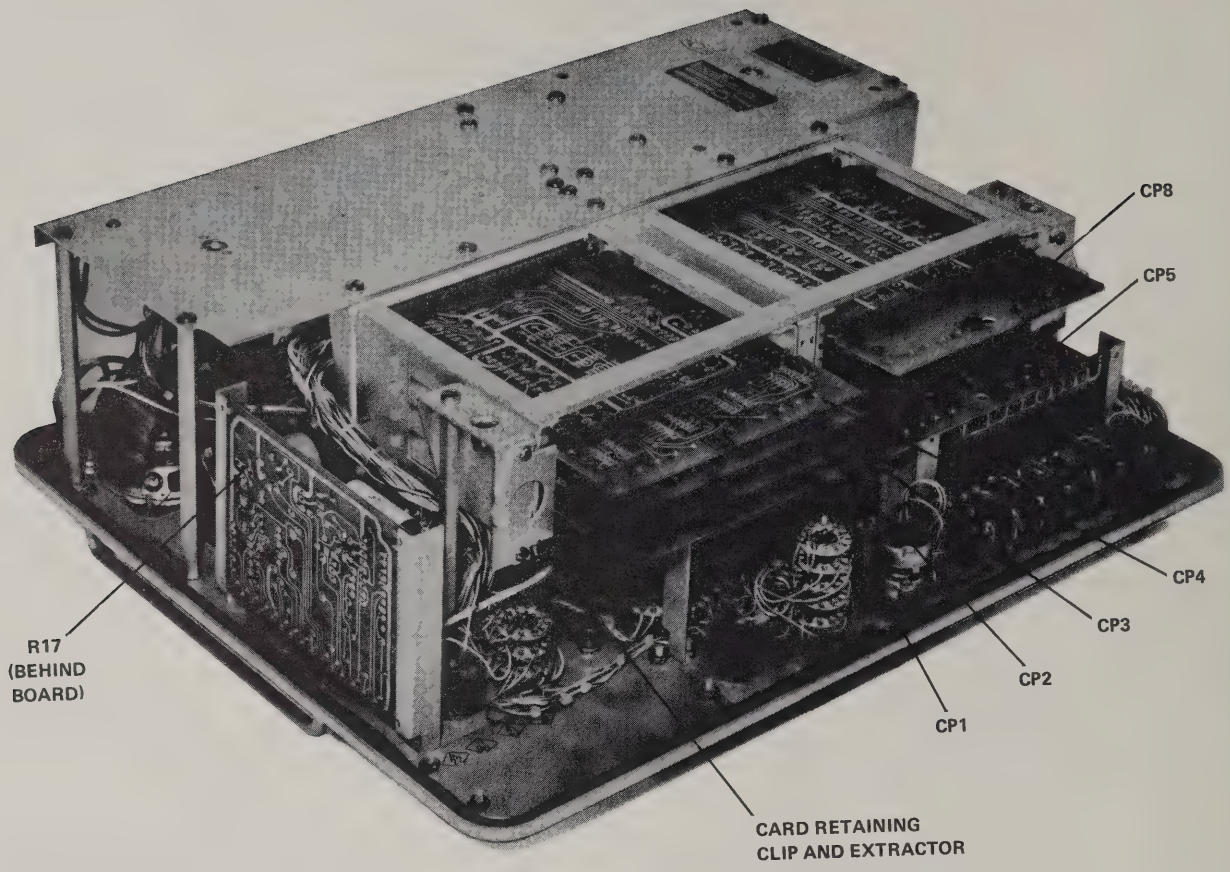


Figure 7-1. Location of Internal Components

CIRCUIT BOARDS

CP1	D02647100 Sierra
CP2	D02648500 Sierra
CP3	D02648600 Sierra
CP4	D02648700 Sierra
CP5	D02648800 Sierra
CP8	D02648900 Sierra

SHORTING PINS

Red	919900046 Sierra
Gray 10 ohms	919900047 Sierra
Green 18 ohms	919900048 Sierra

LENS

White	B0146 Sylvania
Blue	B0143 Sylvania
Red	B0142 Sylvania
Amber	B0140 Sylvania

LAMPS

Power switch	A1G
All others	B0934 Sylvania

7.06 Figure 7-2 shows the orientation of the test points on CP boards 1 through 8. The test points are numbered sequentially 1 through 8, and all exist on each board regardless of whether they are connected to any circuit.

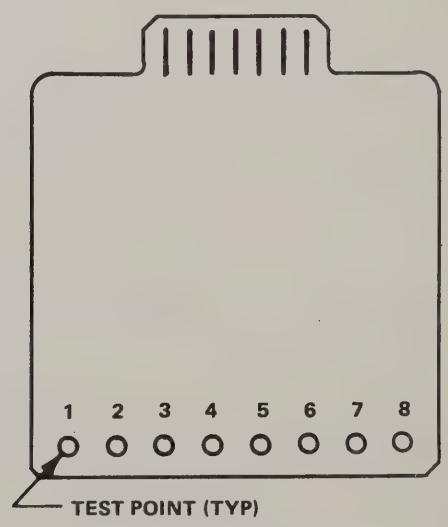


Figure 7-2. CP1 through CP8 Test Point Location

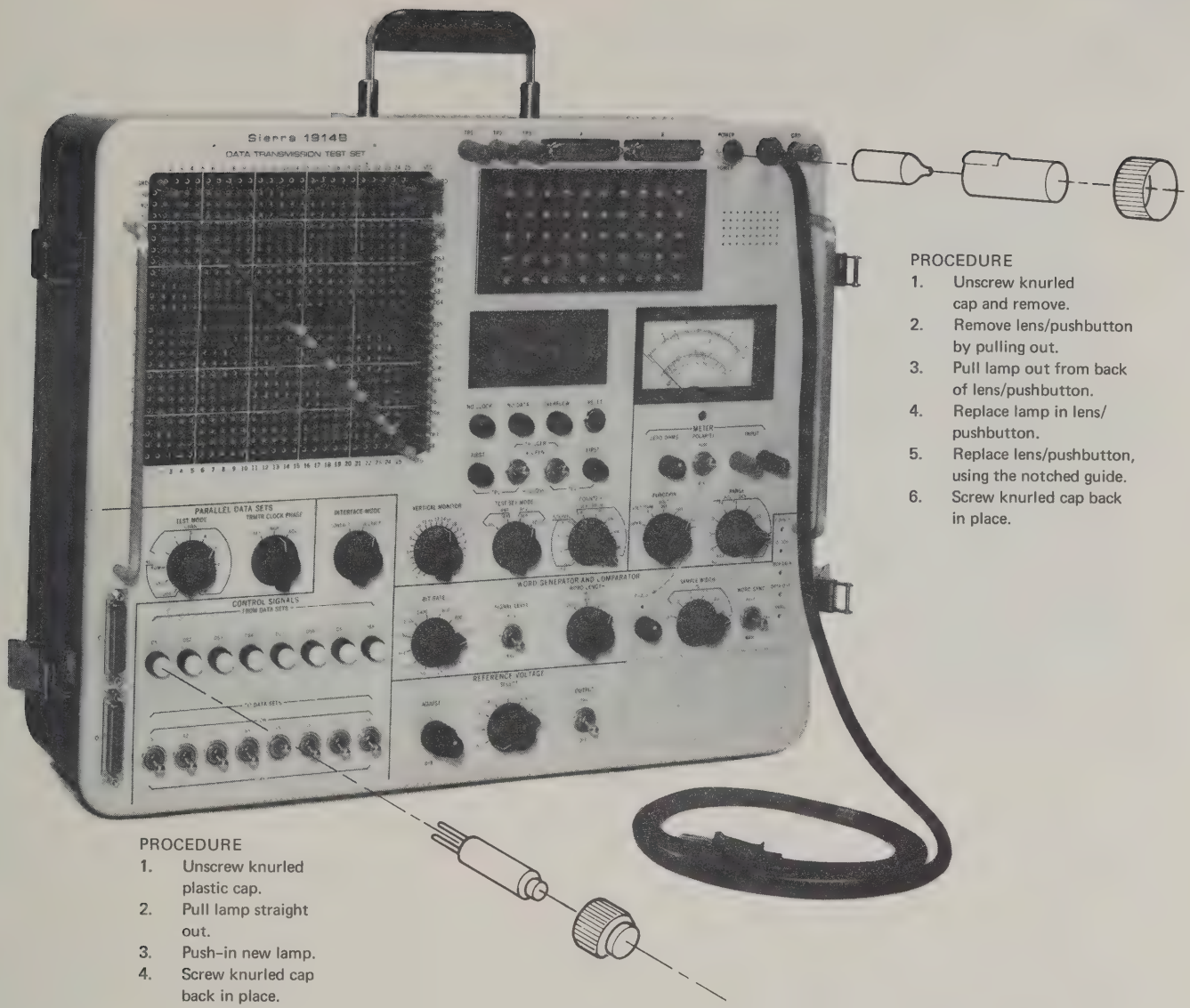

Sierra 1914B
DATA TRANSMISSION TEST SET
PARALLEL DATA SETS
CONTROL SIGNALS
WORD GENERATOR AND COMPARATOR
REFERENCE VOLTAGE
PROCEDURE
1. Unscrew knurled cap and remove.
2. Remove lens/pushbutton by pulling out.
3. Pull lamp out from back of lens/pushbutton.
4. Replace lamp in lens/ pushbutton.
5. Replace lens/pushbutton, using the notched guide.
6. Screw knurled cap back in place.
PROCEDURE
1. Unscrew knurled plastic cap.
2. Pull lamp straight out.
3. Push-in new lamp.
4. Screw knurled cap back in place.

Figure 7-3. Lamp Replacement Procedure

Operational Tests–Single 1914B

7.07 Fuses: By following the procedure shown in Table 7-2, the operator can determine when a fuse has failed. If a fuse is to be replaced, refer to Paragraph 7.04 for access instructions. Figure 7-4 shows the location of fuses and spare fuses.

7.08 Control Signals: Either voltages or contact closures can be used as control signals with the 1914B test set. The procedure shown in Table 7-3 checks the test set for operation with both types of control signals.

7.09 Interval Counter: The procedure shown in Table 7-5 tests the interval counter's ability to detect the first occurrence of a preselected signal transition and also provides a test of the counter display.

7.10 Word Generator and Clock: The procedure shown in Table 7-6 tests the ability of the word generator to produce its three test messages – a dot signal, a 63-bit test message, and a 511-bit test message – and the ability of the clock to generate a timing signal over the range of 150 to 2400 bps.

7.11 Parallel Data Circuits: The procedure shown in Table 7-7 tests the ability of the 1914B to generate the proper type of signals for parallel-data sets.

7.12 Reference Voltages. The procedure shown in Table 7-8 checks the seven fixed voltages and the adjustable voltage from the reference voltage supply.

7.13 Clock Circuits: The procedure shown in Table 7-10 uses an electronic counter to check the clock rates of the 1914B.

7.14 Data and Sample Circuits: In the procedure shown in Table 7-13, the data sync, and clock outputs of the 1914B are checked with the aid of a dual-trace oscilloscope. The dual traces permit checking the phase relationship of the data and clock signals. The oscilloscope must have a variable time base and must be capable of being externally synchronized.

7.15 AC Voltmeter: The procedure shown in Table 7-14 permits calibrating the ac voltmeter with the aid of an external reference signal preferably of 0 dBm level known to be accurate to within 0.1 dB.

Operational Tests—Two Interconnected 1914B's

7.16 The test of Paragraphs 7.17 and 7.18 use two 1914B test sets so interconnected that one serves as the transmitter and the other the receiver.

7.17 Word Generator, Clock, and Sync Circuits: The procedure shown in Table 7-15 checks the data and clock circuits of one 1914B as a transmitter (Set A) and another 1914B as a receiver (Set B).

7.18 Parallel Data Circuits: The procedure shown in Table 7-16 tests the parallel-data mode in both the transmitting and receiving test sets.

Table 7-2

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Operate the POWER switch.	The POWER lamp lights and the set is operative.	1. Fuse F1 2. POWER lamp
2	Set the TEST SET MODE switch to RCV SER, and set the BIT RATE switch to EXT +.	The NO DATA and NO CLOCK lamps light.	1. Fuse F2 2. Defective +23 volt power supply (Fig 6-27)
3	Set the FUNCTION switch to VOLT INT and the RANGE switch to DC/10. Set the SELECT switch to +2.0 and the OUTPUT switch to TP3. Set the VERTICAL MONITOR switch to 1 and the POLARITY switch to NOR. At the matrix, insert a shorting pin in row TP3, column 1.	The meter reads 2.0 volts	1. If the meter reads 0 or is otherwise off in all the plus voltage positions of the SELECT switch, fuse F3 or the +12 power supply may be defective (Fig. 6-27). 2. Pin connections at matrix (6-19). 3. Voltage divider on CP11 (Fig. 6-25). 4. Multiple switch contacts.
4	Set the SELECT switch to –2.0 and POLARITY switch to REV.	Meter reads 2.0 volts	1. If the meter reads 0 or is otherwise off in all of the minus voltage positions of the SELECT switch, fuse F4 or the –12 volt power supply may be defective (Fig. 6-27).
5	Remove the shorting pin in row TP3, column 1.		1. Fuse F5 or faulty +5 volt power supply (Fig. 6-27).
6	Set the FUNCTION switch to VOLT/OHM EXT. Set the one RANGE switch to X1. Short-circuit the INPUT terminals with a test lead. Adjust the ZERO OHMS control.	It should be possible to move the meter pointer to 0 (on ohm-meter scale) with the ZERO OHMs control.	

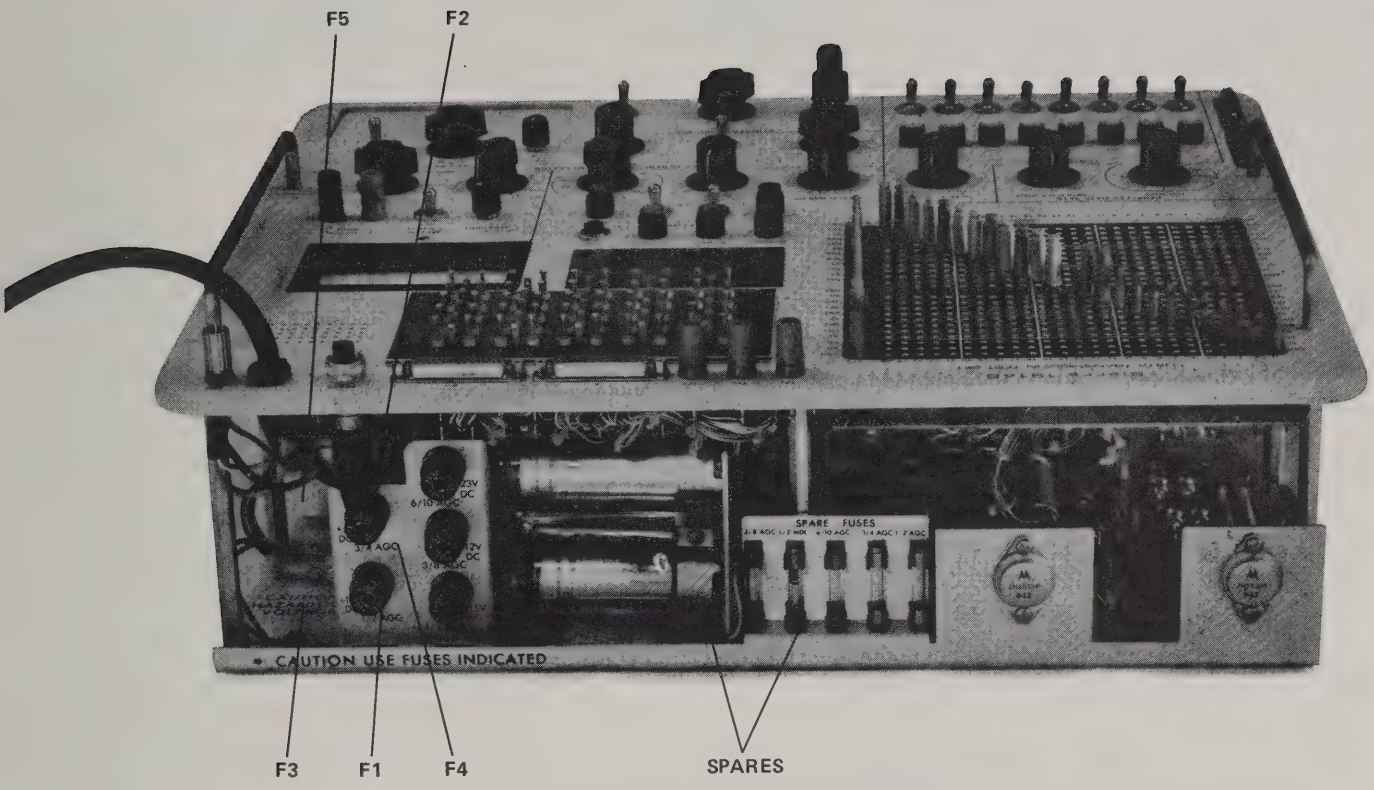


Figure 7-4. Location of Fuses and Spares

Table 7-3

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	At the matrix, insert a shorting pin in row S1, column 1; and insert a second shorting pin in row DS1, column 1. Set toggle switches S1 through S8 to OFF. Operate the POWER switch.	POWER lamp lights	1. POWER lamp 2. Fuse F1
2	Set INTERFACE MODE switch to CONTACT.	Lamps DS1 through DS8 are off.	
3	Set toggle switch S1 to ON.	Lamp DS1 lights.	1. Lamp DS1 (Fig. 6-28). 2. Pin connection on matrix.
4	Set toggle switch S1 to OFF.	Lamp DS1 goes off.	

Table 7-3 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
5	Test the control circuits in accordance with Table 7-4.	Lamps DS2 through DS8 operate as shown in Table 7-4.	1. Lamps DS2 through DS8 or pin connections NOTE: If an indicator lamp fails to light with the INTERFACE MODE switch set to CONTACT, the corresponding position can be tested with the voltmeter. Set the FUNCTION switch to VOLT INT and the RANGE switch to DCV/30, and select the desired matrix connection using the VERTICAL MONITOR switch. The meter will indicate 0 for a lamp failure. If the meter indicates +23 dc volts with the particular S1 through S8 switch set to OFF, the INTERFACE MODE switch or connections may be defective.
6	Repeat steps 1 through 5 with the INTERFACE MODE switch set to VOLTAGE.	Same indications as above.	1. Lamp drivers on CP8 (Fig. 6-28) or ±4. NOTE: If all indicator lamps fail to light with the INTERFACE MODE switch set to VOLTAGE, the corresponding position may be tested with the voltmeter.
7	Set FUNCTION switch to VOLT INT, RANGE to DCV/10, and select the desired matrix connection using the VERTICAL MONITOR switch.	A meter indication of +4.0 ±0.3 dc volts should be observed for toggle switches that are ON and -4.0 ±0.3 dc volts for switches that are OFF.	CP4, CR17 & CR18 (+4v) or CP4, CR19 & CR20 (-4v).
8	Operate the POWER switch.	POWER lamp goes off.	
9	Remove test connections.		

Table 7.4. Operation of Control-Signal Lamps

MATRIX CONNECTIONS		TOGGLE-SWITCH SETTINGS		NORMAL INDICATIONS	
ROW	COLUMN	SWITCH	POSITION	LAMP	CONDITION
DS2	2	S2	ON	DS2	Lighted
S2	2		OFF		Off
DS3	3	S3	ON	DS3	Lighted
S3	3		OFF		Off
DS4	4	S4	ON	DS4	Lighted
S4	4		OFF		Off
DS5	5	S5	ON	DS5	Lighted
S5	5		OFF		Off
DS6	6	S6	ON	DS6	Lighted
S6	6		OFF		Off
DS7	7	S7	ON	DS7	Lighted
S7	7		OFF		Off
DS8	8	S8	ON	DS8	Lighted
S8	8		OFF		Off

Table 7-5

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Set toggle switches S1 through S8 to OFF.		
2	Insert shorting pins in the following matrix positions: row TP1, column 1 row S1, column 1 row TP2, column 2 row S2, column 2.		
3	Turn FUNCTION switch to OFF.		
4	Operate POWER switch.	POWER lamp lights.	
5	Set INTERFACE MODE switch to CONTACT.		
6	Set BIT RATE switch to 2400.		
7	Set TEST SET MODE switch to TRMT SER		
8	Set TRIGGER TP1 and TRIGGER TP2 switches to -/CLOSE.		

Table 7-5 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
9	Set COUNTER switch to INTERVAL/X100.		
10	Momentarily operate the RESET switch.	Counter display reads 00.	1. IC2-4B on CP3 (Fig. 6-22). 2. CP4 (Fig. 6-22). 3. CP9 (Fig. 6-22).
11	Using a suitable timer, set toggle switch S1 to ON.	First TP1 lamp lights, and counter display starts.	1. First TP1 lamp (Fig. 6-21). 2. CP1 oscillator circuit (Fig. 6-20). 3. CP9 (Fig. 6-22). 4. CP4 (Fig. 6-22).
12	After 5 seconds, set toggle switch S2 to ON.	Counter display stopped at approximately 50. FIRST TP1 lamp remains lighted.	5. CP2 (Fig. 6-22).
13	Set TRIGGER TP1 and TRIGGER TP2 switches to +/OPEN.		
14	Momentarily operate the RESET switch.	Counter display reads 00. FIRST TP1 lamp goes out.	
15	Using a suitable timer, set toggle switch S2 to OFF.	FIRST TP2 lamp lights, and counter display starts.	1. FIRST TP2 lamp (Fig. 6-22). 2. CP4 (Fig. 6-22). 3. CP2 (Fig. 6-22).
16	After 5 seconds, set toggle switch S1 to OFF.	Counter display stopped at approximately 50. FIRST TP2 lamp remains lighted.	1. CP4 (Fig. 6-22). 2. CP2 (Fig. 6-22).
17	Operate POWER switch.	POWER lamp goes off.	
18	Remove shorting pins from matrix.		

Table 7-6

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect TP1 to the black INPUT connector and connect TP2 to the red INPUT connector.		
2	Set front-panel controls as follows:		

Table 7-6 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	METER POLARITY SWITCH to REV. TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS. FUNCTION switch to OFF. BIT RATE switch to 1600. SIGNAL LEVEL switch to ±.7V. WORD LENGTH switch to 63. WORD SYNC switch to OFF.		
3	Insert shorting pins in the following matrix positions: row GRD, column 1 row SD, column 2 TP1, column 1 row TP2, column 2.		
4	Operate POWER switch	POWER lamp is lighted.	
5	Set RANGE switch to 1 VAC.		
6	Set FUNCTION switch to VOLT/OHM EXT.	NO DATA lamp is off. NO CLOCK lamp is off.	1. CP4, CP3 (Fig. 6-21). 2. CP2, CP1, CP10 (Fig. 6-20). NOTE: If the NO DATA or NO CLOCK lamps always remain on or off, the most likely failure is with the associated detector on the CP4 board.
		Meter indicates .60 ±0.05 Vac.	1. AC meter circuit (Fig. 6-26). 2. CP3, CP4 (Fig. 6-21).
7	Set WORD LENGTH switch to 511.	Meter indicates .60 ±0.05 Vac.	1. CP10 (Fig. 6-20). 2. CP3 (Fig. 6-21).
8	Set WORD LENGTH switch to DOT.	Meter indicates .75 ±.075 Vac.	1. CP3 (Fig. 6-21). 2. CP10 (Fig. 6-20).

Table 7-6 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
9	Set FUNCTION switch to OFF.		
10	Set BIT RATE switch to 150.		
11	Set WORD LENGTH switch to 63.		
12	Set TEST SET MODE switch to RCV SER.	Counter display indicates counting.	See paragraph 7.09
		NO DATA lamp lights after brief pause.	NO DATA lamp, CP4 (Fig. 6-21).
13	Operate and hold RESET switch.	Counter display reads 00.	See paragraph 7.09.
		OVERFLOW lamp remains off.	CP9 (Fig. 6-22).
14	Release RESET switch.	Counter display counts. OVERFLOW lamp lights when count goes from 99 to 00.	OVERFLOW lamp CP9 (Fig. 6-22).
15	Rotate the BIT RATE switch through all positions (150 – 2400).	Counter display rate increases for each increasing BIT RATE switch position.	CP1, CP2 (Fig. 6-20).
16	Set BIT RATE switch to EXT +.	Counter display stops.	
		NO CLOCK lamp lights after brief pause.	NO CLOCK lamp, CP4 (Fig. 6-21).
17	Set BIT RATE switch to EXT –.	Counter display remains stopped. NO CLOCK lamp remains lighted. NO CLOCK and NO DATA lamps may go out momentarily.	
18	Set FUNCTION switch to VOLT/OHM EXT.		
19	Set the TEST SET MODE switch to TRMT SER.	NO CLOCK lamp remains lighted. May go out momentarily.	
		NO DATA lamp remains lighted. May go out momentarily.	
20	Set the RANGE switch to DCV/1.	Meter indicates 0.7 ±0.1 dc volts.	CP4 (Fig. 6-21); CP12 (Fig. 6-26)
		NOTE: If meter reads downscale, set POLARITY switch to opposite position.	

Table 7-6 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
21	Operate BIT RATE switch between EXT + and EXT – until proper meter indication is obtained.	Meter reads down-scale.	
22	Set the POLARITY switch to the opposite position.	Meter indicates 0.7 ±.1 dc volts	CP4 (Fig. 6-21); CP12 (Fig. 6-26)
23	Set RANGE switch to DCV/10.		
24	Set the SIGNAL LEVEL switch to ±4V.	Meter indicates 4.0 ±0.5 dc volts.	
25	Operate BIT RATE switch between EXT + and EXT – until proper meter indication is obtained.	Meter reads down-scale.	
26	Set the POLARITY switch to the opposite position.	Meter indicates 4.0 ±0.5 volts.	CP4 (Fig. 6-21); CP12 (Fig. 6-26)
27	Set FUNCTION switch to OFF.		
28	Set SIGNAL LEVEL switch to ±.7V.		
29	Set BIT RATE switch to 1600.		
30	Set RANGE switch to ACV/1.		
31	Set FUNCTION switch to SPKR.	Raspy noise heard in loudspeaker.	Speaker or Q1 on CP12 (Fig. 6-26)
32	Rotate RANGE switch through all ACV positions.	Loudspeaker level increases as switch is rotated ccw.	
33	Operate POWER switch.	POWER lamp goes off.	
34	Remove test connections.		

Table 7-7

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect a lead from the black INPUT terminal to TP1 and connect another lead from the red INPUT terminal to TP2.		
2	Connect the 4-dB pad between TP1 and TP2.		
3	Connect the interface cable between Connector A and Connector D, and connect the second cable between Connector B and Connector C.		
4	Set front-panel controls as follows: TEST MODE switch to ALL DOT. TEST SET MODE switch to TRMT 402. BIT RATE switch to EXT +. SIGNAL LEVEL switch to ±4V. FUNCTION switch to OFF. RANGE switch to ACV/1. WORD LENGTH switch to DOT. COUNTER switch to BIT ERRORS.		
5	Insert shorting pins in the following matrix positions: row GRD, column 25. row TP2, column 25.		
6	Operate POWER switch.	POWER lamp lights.	
7	Set FUNCTION switch to VOLT/OHM EXT.		
8	Insert a shorting pin in matrix row TP1, column 2.	Meter indicate 0.7 to 1.1 volts ac.	CP5, CP8 (Fig. 6-23); CP12 (Fig. 6-26)
9	Repeat Step 8 by removing pin from column 2 and inserting it in columns 3, 4, 5, 7, 8, 9 and 10 successively.	Meter indicates 0.7 to 1.1 volts ac.	CP8 (Fig. 6-23)

Table 7-7 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
10	Remove the shorting pin from matrix row TP1, column 10 and insert it in row TP1, column 6.	Meter indicates 0.5 to 0.75 volts ac.	CP5, CP8 (Fig. 6-23)
11	Set the WORD LENGTH switch to 63.		
12	Set the TEST MODE switch to ALL RDM.		
13	Remove the shorting pin from matrix row TP1, column 6.		
14	Repeat Steps 8 and 9.	Meter indicates 0.4 to 0.9 volts ac. NOTE: Meter pointer "jitters" as result of random test messages.	1. CP5, CP8 (Fig. 6-23). 2. CP2 (Fig. 6-20). 3. CP3 (Fig. 6-21).
15	Set TEST MODE switch to CHAN/1.		
16	Remove shorting pin from matrix row TP1 column 10, and insert it in row TP1, column 2.	Meter indicates 0.35 to 0.7 volts ac.	
17	Set TEST MODE switch to CHAN/2.		
18	Move the shorting pin in matrix row TP1 from column 2 to column 3.	Meter indicates 0.35 to 0.7 volts ac.	
19	Set TEST MODE switch to CHAN/3.		
20	Move the shorting pin in matrix row TP1 from column 3 to column 4.	Meter indicates 0.35 to 0.7 volts ac.	
21	Set TEST MODE switch to CHAN/4.		
22	Move the shorting pin in matrix row TP1 from column 4 to column 5.	Meter indicates 0.35 to 0.7 volts ac.	
23	Set TEST MODE switch to CHAN/5.		

Table 7-7 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
24	Move the shorting pin in matrix row TP1 from column 5 to column 7.	Meter indicates 0.35 to 0.7 volts ac.	
25	Set TEST MODE switch to CHAN/6.	Meter indicates 0.35 to 0.7 volts ac.	
26	Move the shorting pin in matrix row TP1 from column 7 to column 8.		
27	Set TEST MODE switch to CHAN/7.	Meter indicates 0.35 to 0.7 volts ac.	
28	Move the shorting pin in matrix row TP1 from column 8 to column 9.		
29	Set TEST MODE switch to CHAN/8.	Meter indicates 0.35 to 0.7 volts ac.	
30	Move the shorting pin in matrix row TP1 from column 9 to column 10.		
31	Operate POWER switch.	POWER lamp goes off.	
32	Remove all test connections.		

Table 7-8

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Insert a shorting pin in matrix row TP3, column 1.		
2	Set OUTPUT switch to OFF.		
3	Operate POWER switch.	POWER lamp is lighted.	
4	Set FUNCTION switch to VOLT INT.		
5	Set RANGE switch to DCV/10.		

Table 7-8 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
6	Set POLARITY switch to NOR.		
7	Set VERTICAL MONITOR switch to 1.		
8	Set ADJUST controls fully counterclockwise, both coarse (outer) and fine (inner).		
9	Set SELECT switch to ADJ.		
10	Set OUTPUT switch to TP3.	Meter indicates 0 dc volts.	1. Meter zero adjust. 2. Faulty meter. 3. Index on vertical monitor sw.
11	Rotate both coarse and fine ADJUST controls fully cw.	Meter pointer varies smoothly and indicates +10.3 ±0.8 dc volts with both controls fully cw.	1. CP11 (Fig. 6-25). 2. +12-Volt power supply (Fig. 6-27). 3. CP12 (Fig. 6-26).
12	Rotate the fine (small) control fully ccw.	Meter indicates at least 0.5 volt dc less than value read in Step 11.	CP11 (Fig. 6-25).
13	Check each of the SELECT switch settings of Table 7-9.	Meter indications shown in Table 7-9.	1. ±12-volt power supplied (Fig. 6-27). 2. CP12 (Fig. 6-27).
14	Operate POWER switch.	POWER lamp goes off.	
15	Remove test connections.		

Table 7-9. Reference Voltages

RANGE SWITCH SETTING	POLARITY SWITCH SETTING	SELECT SWITCH SETTING	NORMAL METER INDICATION
DCV/3	REV	–2.0	1.90 to 2.10
DCV/1	REV	–1.0	0.95 to 1.05
DCV/1	REV	–477	0.45 to 0.50
DCV/1	———	0	0
DCV/1	NOR	+477	0.45 to 0.50
DCV/1	NOR	+1.0	0.95 to 1.05
DCV/3	NOR	+2.0	1.90 to 2.10
DCV/10	NOR	+7.0	6.65 to 7.35

Table 7-10

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect leads from the CLOCK and GRD terminals of the 1914B to the appropriate input terminals of an electronic counter.		
2	Set front-panel controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS.		
3	Operate POWER switches on both 1914B and counter.	1914B POWER lamp is lighted and counter is turned on. NOTE: Allow the 1914B and counter to warm up for 5 minutes before proceeding.	
4	Set the BIT RATE switch to positions 150 through 2400.	Counter readings should be within the tolerances shown in Table 7-11.	CP1, CP2 (Fig. 6-20)
5	Set the COUNTER switch to each of the four INTERVAL positions.	Counter readings should be within the tolerances shown in Table 7-12.	
6	Set the BIT RATE switch to EXT +.		
7	Set the COUNTER switch to BIT ERRORS.		
8	Set the TEST SET MODE switch to TRMT 402.	Counter should read 75 ±4 Hz.	CP5
9	Operate the POWER switches at both the 1914B and counter.	POWER lamp goes off and counter is turned off.	

Table 7-11. Bit Rate Test

BIT RATE SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY (Hz)
150	150 ±5
300	300 ±9
600	,600 ±18
1,000	1,000 ±30
1,200	1,200 ±36
1,400	1,400 ±42
1,600	1,600 ±48
1,800	1,800 ±54
2,000	2,000 ±60
2,400	2,400 ±72

Table 7-12. Counter Test

COUNTER INTERVAL SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY (Hz)
X .1	10,000 ±250
X 1	1,000 ±25
X 10	100 ±3.0
X 100	10 ±0.3

Table 7-13

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the oscilloscope to the 1914B as follows: Connect the channel 1 oscilloscope probe to the CLOCK test point on the 1914B. Connect the channel 2 oscilloscope probe and the oscilloscope SYNC lead to the SYNC test point on the 1914B. Connect a lead from the GRD terminal of the 1914B to the ground terminal of the oscilloscope.		
2	Set the 1914B front-panel controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS. BIT RATE switch to 1000. SIGNAL LEVEL switch to ±4v. WORD LENGTH switch to 63. SAMPLE WIDTH switch to .5μs.		

Table 7-13 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
3	Operate the POWER switches on both the 1914B and the oscilloscope.	POWER lamp lights and the oscilloscope turns on.	
4	Set the oscilloscope controls to observe the channel 2 input using external sync on the oscilloscope.	Observe waveform A, Figure 7-5.	1. CP4 (Fig. 6-22). 2. CP3 (Fig. 6-21). 3. CP2 and CP1 (Fig. 6-20).
5	Set the oscilloscope controls to observe the channel 1 input using external sync on the oscilloscope.	Observe waveform B, Figure 7-5.	CP2 (Fig 6-20).
6	Set the WORD LENGTH switch to 511.		
7	Set the oscilloscope controls to observe the channel 1 input first and then the channel 2 input.	Waveforms observed in Steps 4 and 5 do not change.	CP3 (Fig. 6-21)
8	Transfer the two connections at the SYNC test point of the 1914B to the DATA OUT test point.		
9	Set the oscilloscope controls to observe channel 1 and 2 inputs simultaneously using external sync.	Observe waveforms C, Figure 7-5.	CP3 (Fig. 6-21).
10	Set the WORD LENGTH switch to 63.	Observe waveforms D, Figure 7-5.	CP3 (Fig. 6-21).
11	Set the WORD LENGTH switch to DOT.	Using internal sync at the oscilloscope, observe waveform E, Figure 7-5.	CP3 (Fig. 6-21).
12	Disconnect the oscilloscope probe from the CLOCK jack. With the ac power off; remove the test set case (paragraph 7.04) and reapply ac power. Connect the oscilloscope lead to test point TP1 of circuit pack CP2 (see Paragraph 7.06 and Figure 7-2.		

Table 7-13 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
13	Remove the oscilloscope sync lead from the 1914B SYNC terminal and connect it to the CLOCK jack.	On channel 1 of the oscilloscope, observe a very narrow positive pulse at center of display.	CP3
14	Using external sync, set the oscilloscope controls to adjust time base so that one bit interval of the data signal occupies a 10-cm sweep on the graticule.	NOTE: It may be necessary to increase the beam intensity to view the pulse. Observe on the oscilloscope screen that the pulse width of the channel 1 input is within ±4% of the value marked on each SAMPLE WIDTH switch position.	CP1 (Fig. 6-20).
15	Turn the SAMPLE WIDTH switch to each of its % positions (10% through 50%).	Each pulse is centered within 2% along the vertical axis of the oscilloscope. POWER lamp is turned off and the oscilloscope is turned off.	
16	Operate both the 1914B and oscilloscope POWER switches.		
17	Remove test connections. Unplug unit and mount it back in its case.		

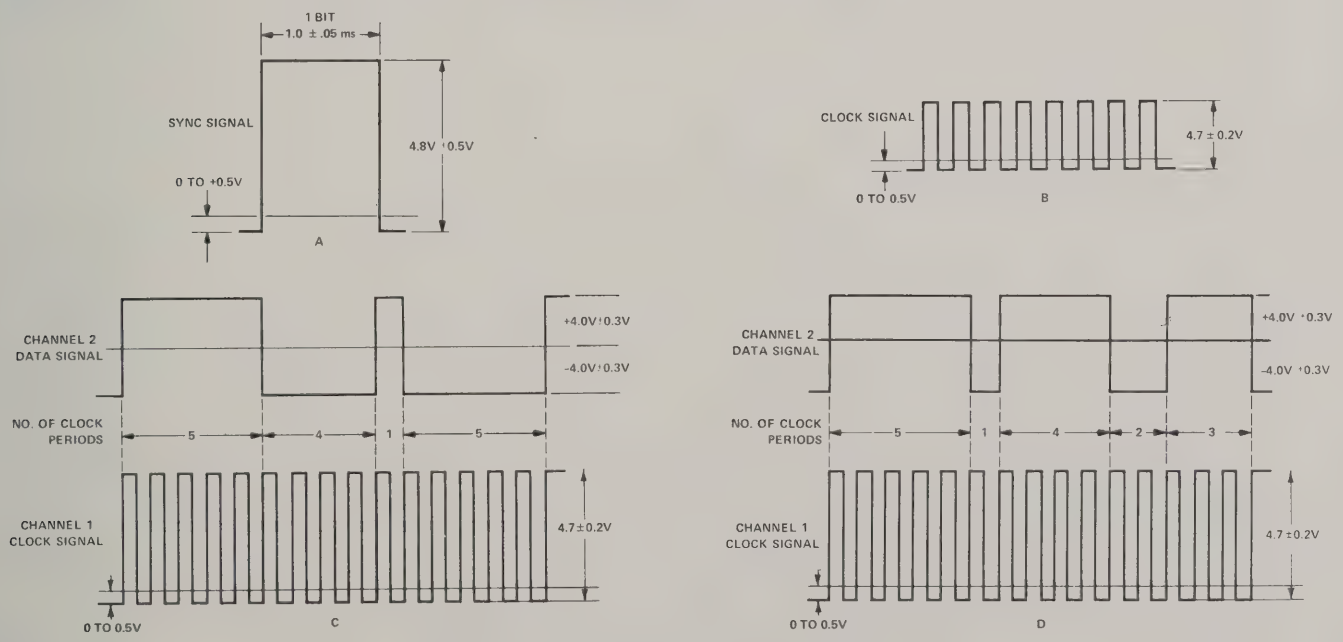


Figure 7-5. Data and Sample Circuit Waveforms

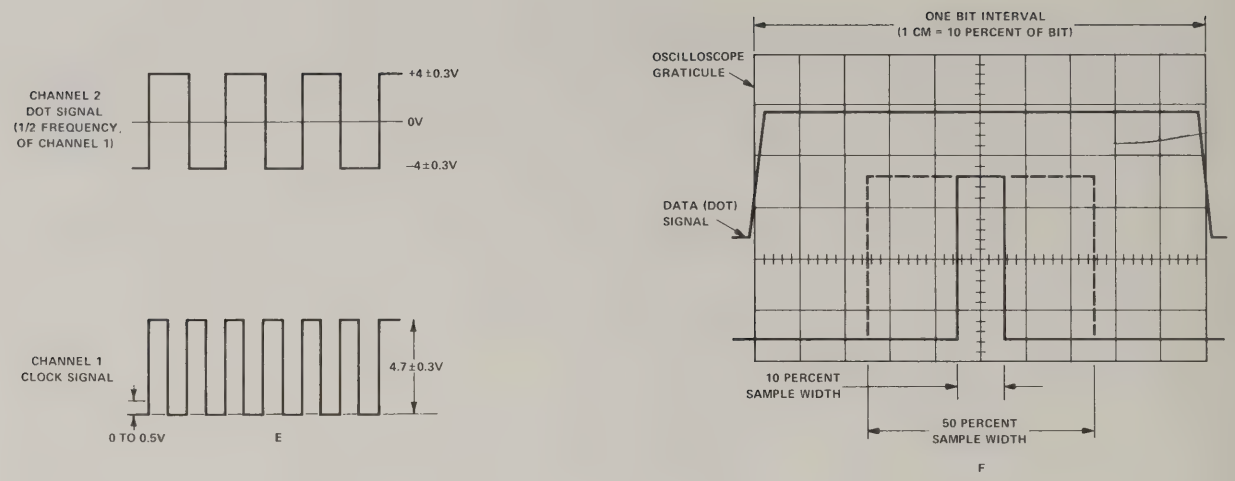


Figure 7-5. Data and Sample Circuit Waveforms (Cont)

Table 7-14

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the output of the reference generator to the INPUT terminals of the 1914B.		NOTE: This AC meter circuit has a 600Ω input impedance. The preferred input is a 0 dbm/600Ω signal at 1000 Hz.
2	Turn on the signal generator and set its output to some known value within the ac volts range of the 1914B meter.		
3	Operate the 1914B POWER switch.		
4	Turn the 1914B FUNCTION switch to VOLT/OHM EXT.		
5	Set the 1914B RANGE switch to the highest ac range that will permit the nearest full-scale meter deflection.		
6	If the meter reading is not the same as the known input voltage, remove the rear cover of the 1914B as described in Paragraph 7.04 and adjust R17 (Figure 7-1) until the meter reading agrees with the known voltage.		
7	Remove test connections.		
8	Turn power off.		

Table 7-15

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the interface cable from Connector A on Set A (transmitter) to Connector A on Set B (receiver).		
2	On the front panel of Set A, set the controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS. BIT RATE switch to 150. SIGNAL LEVEL switch to ±4V. WORD LENGTH switch to 63.		
3	In the matrix of Set A, insert a shorting pin in the following position: row GRD, column 1		
4	On the front panel of Set B, set the controls as follows: TEST SET MODE switch to RCV SER. COUNTER switch to BIT ERRORS. FUNCTION switch to PHASE ADJ. BIT RATE switch to 150. SIGNAL LEVEL switch to ±4V. WORD LENGTH switch to 63. SAMPLE WIDTH switch to .5 μs. WORD SYNC switch to OFF.		

Table 7-15 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
5	In the matrix of Set B, insert shorting pin in the following positions: row GRD, column 1 row RD, column 2		
6	Operate the POWER switches on both sets.	POWER lamps light.	
7	In the matrix of Set A, insert a shorting pin in row SD, column 2.	Set B meter pointer deflects. The NO DATA and NO CLOCK lamps go off. Counter display starts.	1. Matrix connections. 2. See paragraph 7.07 through 7.10.
8	Adjust the Set B PHASE control.	Set B meter pointer nulls to zero.	
9	Turn the Set B FUNCTION switch to OFF.		
10	Momentarily operate the Set B WORD SYNC switch to MAN.	Set B counter display stops.	
11	Turn the Set A WORD LENGTH switch to 511, then return to 63.	Set B counter display starts.	
12	Set the Set B WORD SYNC switch to AUTO.	Set B counter display stops.	
13	Depress RESET button.	Display shows 00, OVERFLOW lamp is off.	
14	Set the WORD LENGTH switches on both test sets to 511.	Set B counter display may run momentarily, then stop.	
15	Set the BIT RATE switches of both test sets to 300.		
16	Set the Set B FUNCTION switch to PHASE ADJ.		
17	Adjust the Set B PHASE control for zero indication.	Meter pointer indicates zero.	
18	Set the Set B FUNCTION switch to OFF.	Counter display may run momentarily, then stop.	

Table 7-15 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
19	Repeat Steps 15 through 18 for each BIT RATE switch position through 2400.	Same as in Steps 15 through 18.	
20	Set the Set B WORD SYNC switch to OFF.		
21	Set the Set A WORD LENGTH switch to 63.		
22	Set the Set B COUNTER switch to BLOCK ERRORS/WL.	The Set B counter display runs at a slower rate.	
23	Turn the Set B COUNTER switch to each BLOCK ERROR position through 16 WL.	The counter display runs at a decreasing rate for each increase in block length.	
24	Operate the POWER switches of both test sets.	POWER lamps are turned off.	
25	Remove all test connections. NOTE: The two 1914B's should now be exchanged and the above tests rerun so that the transmitting and receiving functions of both sets will be tested.		

Table 7-16

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect a test cable from Connector C on Set A (transmitter) to Connector D on Set B (receiver).		1. Matrix Connections 2. See paragraph 7.07 through 7.11.
2	On the front panel of Set A, set the controls as follows: TEST MODE switch to ALL RDM. WORD LENGTH switch to 63. TRMTR CLOCK PHASE switch to ADV. SIGNAL LEVEL switch to ±4V.		

Table 7-16 (Cont)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
2 (Cont)	TEST SET MODE switch to TRMT 402. COUNTER switch to BIT ERRORS. BIT RATE switch to EXT +.		
3	On the front panel of Set B, set the controls as follows: TEST MODE switch to ALL RDM. TEST SET MODE switch to RCV 402. WORD LENGTH switch to 63. SIGNAL LEVEL switch to ±4V. TRMTR CLOCK PHASE switch to NOR. COUNTER switch to BIT ERRORS. BIT RATE switch to EXT –. WORD SYNC switch to OFF.		
4	Operate the POWER switches on both test sets.	POWER lamps light. Set B counter display runs.	
5	Momentarily operate set B WORD SYNC switch to MAN.	Set B counter display stops.	
6	Set TEST MODE switches on both sets to CHAN 1. Then momentarily operate Set A WORD LENGTH switch to 511 and back to 63.	Set B counter display will run.	
7	Momentarily operate Set B WORD SYNC switch to MAN.	Set B counter display stops.	
8	Repeat Steps 6 and 7 for TEST MODE/CHAN switch positions 2 through 8.	Same as Steps 6 and 7.	
9	Operate POWER switches on both test sets.	POWER lamps go off.	
10	Remove all test connections. NOTE: The two 1914B's should now be exchanged and the above tests rerun so that the transmitting and receiving functions of both sets will be tested.		

SECTION 8
REPLACEABLE PARTS LIST

8.01 Standard components have been used in this instrument whenever possible. Both standard and special components may be ordered direct from the factory. When ordering parts, always include:

1. Sierra Stock number.
2. Circuit reference designation and commercial description.
3. Name, model, and serial number of the instrument.

8.02 Parts for this instrument, or further service information, may be obtained from:

SIERRA ELECTRONIC OPERATION
Philco-Ford Corporation
3885 Bohannon Drive
Menlo Park, California 94025

Telephone–(415) 322-7222
TWX–910-373-1282

Table 8-1. Manufacturer's Supply Codes

Code	Manufacturer's Name and Address
00348	Microtran Co. Inc., 145 E. Mineola Ave., Valley Stream, N.Y. 11582
01121	Allen Bradley Co., 1201 S. 2nd St., Milwaukee, Wis. 53204
04426	Illinois Tool Works, 6615 W. Irving Park Rd., Chicago, Ill. 60634
04713	Motorola Semiconductor Products Inc., 5005 East McDowell Road, Phoenix, Ariz. 85008
05276	Pomona Electronics Co., Inc., 1500 East 9th, Pomona, Calif. 91766
07263	Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corp., 464 Ellis St., Mountain View, Calif. 94040
07397	Sylvania Electronics, Sylvania Electronic Systems Western Division, 500 Evelyn Ave., Mountain View, Calif. 94040
08779	Signal Transformer Co., Inc., 1 Junius St., Brooklyn, N.Y. 11212
12065	Transitron Electronic Corp., 144 Addison St., East Boston, Mass.
13103	Thermalloy Co., 8717 Diplomacy Row, Dallas, Tex. 75247
15605	Culterhammer, Inc., Milwaukee, Wisc.
16299	Corning Glass Works Electronic Components Division, 3900 Electronics Drive, Raleigh, N C 27604
16770	Burroughss Corp., Pasadena Plant, Pasadena, Calif.
17870	Daven Division Thomas Edison Ind., McGraw Edison Co., Greiner Field Municipal Airport, Manchester, Manchester, N.H. 03103
28869	Quincy Speaker Mfg. Co., 219 Oak Street, Quincy, Ill. 62301
47904	Polaroid Corp., 730 Main, Cambridge, Mass. 02139
49956	Raytheon Co., Lexington, Mass. 02173
56289	Sprague Electric Co., North Adams, Mass. 01247
58474	Superior Electric Co., 383 Middle St., Bristol, Conn. 06010

Table 8-1. Manufacturer's Supply Codes

Code	Manufacturer's Name and Address
65092	Weston Instruments Inc., Weston Newark, Newark, N.J.
70903	Beldon Corp, 415 S. Kilpatrick, Chicago, Ill. 60644
71400	Bussman Mfg. Division of McGraw Edison Co., 2536 W. University St., St. Louis, Mo. 63017
71590	Globe Union, Inc., Centralab Division, P.O. Box 591, Milwaukee, Wis. 53201
73293	Hughes Ai rcraft Co., Electron Dynamics Div., P.O. Box 2999, Torrance, Calif. 90509
75915	Littelfuse, Inc., 800 E. Northwest Hwy., Des Plaines, Ill. 60016
76854	Oak Mfg. Co. Div. of Oak Electro/netics Corp., S. Main Street, Crystal Lake, Ill. 60014
91637	Dale Electronics Inc., P.O. Box 609, Columbus, Nebr. 68601
93790	Cornelldubilier Electronics Division, Federal Pacific Electric Co., 1605 Rodney French Blvd., New Bedford, Mass. 02741
94668	Philco-Ford Corp., Sierra Electronics Division, 3885 Bohannon Drive, Menlo Park, Calif. 94025
98291	Sealectro Corp., 225 Hoyt, Mamaroneck, N.Y. 10544
98376	Zero Mfg Co., West Division, 1121 Chestnut St., Burbank, Ca. 91503

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	SIERRA 1914B DATA TRANSMISSION TEST SET	C02646101				
	COVER ASSEMBLY	D02646201	94668	D02646201	1	
	CASE ASSEMBLY	D02646901	94668	D02646901	1	
	PANEL ASSEMBLY	D02807601	94668	D02807601	1	
	TEST LEAD,BLACK	916400034	05276	1959-55	1	
	TEST LEAD, RED	916400035	05276	1959-55	1	
	ENCAPSULATED 4-DB PAD	919900042	94668	C02695400	1	
	INTERFACE CABLE ASSEMBLY	919900043	94668	C02695500	2	
	SHORTING PIN,RED	919900046	98291	0772-002-27-2	31	
	PROGRAMING PIN	919900047	98291	623-004	9	
	PROGRAMING PIN	919900048	94668	B02693000	9	
	COVER ASSEMBLY	D02646201	94668	C02646201		
	SHIM-STRIKE	B02646600	94668	B02646600	4	
	PANEL ASSEMBLY	D02807601	94668	D02807601		
	PANEL ASSEMBLY	C02807501	94668	C02807501	1	
	WINDOW,NIXIE,PLEXIGLASS,LAMINATED, NON-GLARE,AMBER	919800024	47904	FACP24	1	
	WINDOW,NIXIE,PLEXIGLASS,LAMINATED, NON-GLARE,AMBER	919800024	47904	FACP24	1	
CP1	CP1 PRINTED CIRCUIT BOARD ASSEMBLY	D02648400	94668	C02648400	1	
CP2	CP2 PRINTED CIRCUIT BOARD ASSEMBLY	D02648500	94668	C02648500	1	
CP3	CP3 PRINTED CIRCUIT BOARD ASSEMBLY	D02648600	94668	C02648600	1	
CP4	CP4 PRINTED CIRCUIT BOARD ASSEMBLY	D02648700	94668	D02648700	1	
CP5	CP5 ASSEMBLY	D02648800	94668	D02648800	1	
CP8	CP8 ASSEMBLY	D02648900	94668	D02648900	1	
	CP1 PRINTED CIRCUIT BOARD ASSEMBLY	D02648400	94668	C02648400		
	PRINTED CIRCUIT BOARD	904500402	94668	904500402	1	
C1	CAPACITOR,FXD,ELECTROLYTIC,100MFD,6V, PERM 10 PCT, SOLID TANTALUM, SLEEVED	902710107	56289	150D107X9006R2	1	
C2	CAPACITOR,FXD,GLASS,0.0047MFD,50V, PERM 10 PCT, AXIAL LEAD	902900472	16299	CYK01BT472K	1	
C3	CAPACITOR,FXD,MICA,200PF,300V,PERM 5 PCT,	901900201	93790	CD7FC201J03	1	
C4	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PERM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C5	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PERM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C6	CAPACITOR,FXD,ELECTROLYTIC,5MFD,6V,PERM 5PCT,SOLID TANTALUM,SLEEVED	902710505	56289	151D5C5X5006X2	1	
C7	CAPACITOR,FXD,GLASS,0.01MFD,50V,PERM 10 PCT,AXIAL LEAD	902900103	16299	CYK01BT103K	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
C8	CAPACITOR,FXD,MYLAR,C.C245MFD,2COV,PCRM 1 PCT	901102452	56289	420P116	1	
C9	CAPACITOR,FXD,ELECTROLYTIC,1MFD,15V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902730105	56289	150D1C5X9015A2	1	
C10	CAPACITOR,FXD,MICA,20CPF,300V,PORM 5 PCT,	901900201	93790	CD7FC201J03	1	
C11	CAPACITOR,FXD,MICA,200PF,30CV,PORM 5 PCT,	901900201	93790	CD7FC201J03	1	
C12	CAPACITOR,FXD,ELECTROLYTIC,1CCMFD,6V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902710107	56289	150D107X9006R2	1	
C13	CAPACITOR,FXD,ELECTROLYTIC,1CCMFD,20V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720107	56289	150D107X9020S2	1	
C14	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C15	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C16	CAPACITOR,FXD,GLASS,0.0C1MFD,50V,PCRM 10PCT,AXIAL LEAD	902900102	16299	CYK01BT102K	1	
C17	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C18	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C19	CAPACITOR,FXD,GLASS,0.01MFD,5CV,PCRM 10 PCT,AXIAL LEAD	902900103	16299	CYK01BT103K	1	
C20	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C21	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C22	CAPACITOR,FXD,ELECTROLYTIC, 1UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C23	CAPACITOR,FXD,ELECTROLYTIC,1MFD,10V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720105	56289	150D105X9010A2	1	
C24	CAPACITOR,FXD,ELECTROLYTIC, 47UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902720476	56289	150D476X9020R2	1	
CR1	DIODE	910500101	12065	1N3666	1	
CR2	DIODE	910500101	12065	1N3666	1	
CR3	DIODE	910500098	04713	1N816	1	
CR4	DIODE	910500102	07263	1N753A	1	
CR5	DIODE	910500100	07263	1N4610	1	
CR6	DIODE	910500103	07263	1N914	1	
CR7	DIODE	910500102	07263	1N753A	1	
CR8	DIODE	910500097	04713	1N3828A	1	
CR9	DIODE	910500100	07263	1N4610	1	
CR10	DIODE	910500100	07263	1N4610	1	
CR11	DIODE	910500103	07263	1N914	1	
CR12	DIODE	910500103	07263	1N914	1	
IC10-1	INTEGRATED CIRCUIT	920300062	07263	U5B770939X	1	
IC11-1	INTEGRATED CIRCUIT	920300061	07263	U5B771039X	1	
IC11-2	INTEGRATED CIRCUIT	920300061	07263	U5B771039X	1	
IC11-3	INTEGRATED CIRCUIT	920300061	07263	U5B771039X	1	
Q1	TRANSISTOR	910300091	04713	2N3250	1	
Q2	TRANSISTOR	910300091	04713	2N3250	1	
Q3	TRANSISTOR	910300090	04713	2N718	1	
Q4	TRANSISTOR	910300089	04713	2N956	1	
Q5	TRANSISTOR	910300089	04713	2N956	1	
R1	RESISTOR,FXD,FILM,20.5KCHMS,1/8W,PCRM 1 PCT,METAL FILM	907300108	16299	MA55	1	
R2	RESISTOR,FXD,FILM,9.53KCHMS,1/8W, PORM 1 PCT,METAL FILM	907300065	16299	MA55	1	
R3	RESISTOR,FXD,FILM,5110HMS,1/4W,PORM 1 PCT,METAL FILM	908300108	16299	MA60	1	
R4	RESISTOR,FXD,FILM,19.6KCHMS,1/8W,PCRM 1 PCT,METAL FILM	907300106	16299	MA55	1	
R5	RESISTOR,FXD,FILM,1.47KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300076	16299	MA55	1	
R6	RESISTOR,FXD,FILM,5110HMS,1/8W,PORM 1 PCT,METAL FILM	907300071	16299	MA55	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R7	RESISTOR,FXD,FILM,3010HMS,1/4W,PORM 1 PCT, METAL FILM	908300107	16299	MA60	1	
R8	RESISTOR,FXD,FILM,2.37KCHMS,1/8W, PORM 1 PCT,METAL FILM	907310013	16299	MA55	1	
R9	RESISTOR,FXD,FILM,3.14KCHMS,1/8W, PORM 1 PCT,METAL FILM	907300082	16299	MA55	1	
R10	RESISTOR,FXD,FILM,1CCOHMS,1/8W,PORM 1 PCT,METAL FILM	907310021	16299	MA55	1	
R11	RESISTOR,FXD,FILM,20CHMS,1/4W,PORM 1 PCT, METAL FILM	908300102	16299	MA60	1	
R12	RESISTOR,FXD,FILM,1KCHMS,1/4W,PORM 1 PCT, METAL FILM	908310007	16299	MA60	1	
R13	RESISTOR,FXD,COMPOSITION,56CCHMS,1/2W, PORM 5 PCT	905010561	01121	EB1-2-561J	1	
R14	RESISTOR,FXD,FILM,46.4KCHMS,1/8W,PORM 1 PCT METAL FILM	907300113	16299	MA55	1	
R15	RESISTOR,FXD,FILM,36.5KCHMS,1/8W, PORM 1 PCT,METAL FILM	907300112	16299	MA55	1	
R16	RESISTOR,FXD,COMPOSITION,5.6KOHMS, 1/4W,PORM 5 PCT	906910562	01121	CB1-4-5601J	1	
R17	RESISTOR,FXD,COMPOSITION,360CCOHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R18	RESISTOR,FXD,FILM,31.6KCHMS,1/8W, PORM 1 PCT,METAL FILM	907300111	16299	MA55	1	
R19	RESISTOR,FXD,FILM,147KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300118	16299	MA55	1	
R20	RESISTOR,FXD,COMPOSITION,5100HMS,1/4W, PORM 5 PCT	906900511	01121	CB1-4-511J	1	
R21	RESISTOR,FXD,FILM,2870CHMS,1/4W,PORM 1 PCT,METAL FILM	908300109	16299	MA60	1	
R22	RESISTOR,FXD,FILM,4990CHMS,1/4W,PORM 1 PCT,METAL FILM	908300111	16299	MA60	1	
R23	RESISTOR,FXD,FILM,10C0CHMS,1/8W,PORM 1 PCT,METAL FILM	907300073	16299	MA55	1	
R24	RESISTOR,FXD,FILM,4990CHMS,1/8W,PORM 1 PCT, METAL FILM	907300090	16299	MA55-4991F	1	
R25	RESISTOR,FXD,FILM,3320CHMS,1/8W,PORM 1 PCT,METAL FILM	907300083	16299	MA55	1	
R26	RESISTOR,FXD,FILM,10C0OHMS,1/8W,PORM 1 PCT,METAL FILM	907300073	16299	MA55	1	
R27	RESISTOR,FXD,FILM,10C0CHMS,1/8W,PORM 1 PCT,METAL FILM	907300073	16299	MA55	1	
R28	RESISTOR,FXD,FILM,33200HMS,1/4W,PORM 1 PCT,METAL FILM	908300110	16299	MA60	1	
R29	RESISTOR,FXD,FILM,4220HMS,1/8W,PORM 1 PCT,METAL FILM	907300070	16299	MA55	1	
R30	RESISTOR,FXD,FILM,41.2OHMS,1/8W, PORM 1 PCT, METAL FILM	907300066	16299	MA55	1	
R31	RESISTOR,FXD,FILM,82.5CHMS,1/8W,PORM 1 PCT,METAL FILM	907310018	16299	MA55	1	
R32	RESISTOR,FXD,FILM,165OHMS,1/8W, PORM 1 PCT, METAL FILM	907300067	16299	MA55	1	
R33	RESISTOR,FXD,FILM,332OHMS,1/8W,PORM 1 PCT, METAL FILM	907300069	16299	MA55	1	
R34	RESISTOR,FXD,FILM,6490HMS,1/8W PORM 1 PCT,METAL FILM	907300072	16299	MA55	1	
R36	RESISTOR,FXD,FILM,196OHMS,1/4W,PORM 1 PCT,METAL FILM	908300105	16299	MA60	1	
R37	RESISTOR,FXD,FILM,2C5OHMS,1/4W,PORM 1 PCT,METAL FILM	908300106	16299	MA60	1	
R38	RESISTOR,FXD,COMPOSITION,560CHMS,1/2W, PORM 5 PCT	905010561	01121	EB1-2-561J	1	
R39	RESISTOR,FXD,WW,820HMS,3W,PORM 5 PCT	906200820	09746	3X	1	
R40	RESISTOR,FXD,FILM,3010HMS,1/4W,PORM 1 PCT, METAL FILM	908300107	16299	MA60	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R40	RESISTOR,FXD,FILM,1620HMS,1/4W,PORM 1 PCT, METAL FILM	908300123	16299	MA60	1	
R40	RESISTOR,FXD,FILM,422OHMS,1/4W,PORM 1 PCT, METAL FILM	908300124	16299	MA60	1	
	CP2 PRINTED CIRCUIT BOARD ASSEMBLY	D02648500	94668	D02648500		
	PRINTED CIRCUIT BOARD	904500403	94668	904500403	1	
C5	CAPACITOR,FXD,MICA,100PF,300V,PORM 5 PCT	901920101	93790	CD6FC101J03	1	
C6	CAPACITOR,FXD,MICA,100PF,300V,PORM 5 PCT	901920101	93790	CD6FC101J03	1	
C7	CAPACITOR,FXD,MICA,82PFD,300V,PORM 5 PCT	901910820	93790	CD6EC820J03	1	
C8	CAPACITOR,FXD,ELECTROLYTIC,1MFD,10V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720105	56289	150D105X9010A2	1	
C9	CAPACITOR,FXD,ELECTROLYTIC, 1UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C11	CAPACITOR,FXD,MICA,100PF,300V,PORM 5 PCT	901920101	93790	CD6FC101J03	1	
C12	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C30	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C31	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C40	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C41	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C1.0	CAPACITOR,FXD,GLASS,0.027MFD,50V, PORM 10 PCT, AXIAL LEAD	902900273	16299	CYK02BU273K	1	
C1.1	CAPACITOR,FXD,GLASS,0.027MFD,50V, PORM 10 PCT, AXIAL LEAD	902900273	16299	CYK02BU273K	1	
C2.0	CAPACITOR,FXD,GLASS,0.056MFD,50V,PORM 10 PCT,AXIAL LEAD	902900563	16299	CYK02BV563K	1	
C2.1	CAPACITOR,FXD,GLASS,0.056MFD,50V,PORM 10 PCT,AXIAL LEAD	902900563	16299	CYK02BV563K	1	
C10.0	CAPACITOR,FXD,MICA,270PF,300V,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C10.1	CAPACITOR,FXD,MICA,270PF,300V,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
CR3	DIODE	910500103	07263	1N914	1	
CR4	DIODE	910500103	07263	1N914	1	
CR5	DIODE	910500101	12065	1N3666	1	
CR6	DIODE	910500101	12065	1N3666	1	
CR9	DIODE	910500101	12065	1N3666	1	
CR10	DIODE	910500101	12065	1N3666	1	
CR1.0	DIODE	910500098	04713	1N816	1	
CR1.1	DIODE	910500098	04713	1N816	1	
CR2.0	DIODE	910500098	04713	1N816	1	
CR2.1	DIODE	910500098	04713	1N816	1	
CR7.2	DIODE	910500101	12065	1N3666	1	
CR7.3	DIODE	910500101	12065	1N3666	1	
CR8.2	DIODE	910500103	07263	1N914	1	
CR8.3	DIODE	910500103	07263	1N914	1	
IC1-1	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC1-2	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC2-1	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC2-2	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC4-1	INTEGRATED CIRCUIT	920300070	07263	U6A994159X	1	
IC5-1	INTEGRATED CIRCUIT	920300067	07263	U6A994559X	1	
IC11-0	INTEGRATED CIRCUIT	920300061	07263	U5B771039X	1	
IC11-1	INTEGRATED CIRCUIT	920300061	07263	U5B771039X	1	
Q1.2	TRANSISTOR	910300090	04713	2N718	1	
Q1.3	TRANSISTOR	910300090	04713	2N718	1	
R9	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R10	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R11	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R12	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R13	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R14	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R15	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R16	RESISTOR,FXD,FILM,1.21KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300074	16299	MA55	1	
R17	RESISTOR,FXD,COMPOSITION,3600OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R18	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R19	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R20	RESISTOR,FXD,COMPOSITION,5.6KOHMS, 1/4W,PORM 5 PCT	906910562	01121	CB1-4-5601J		
R24	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R25	RESISTOR,FXD,COMPOSITION,36000OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R26	RESISTOR,FXD,COMPOSITION,2000OHMS,1/4W, PORM 5 PCT	906910202	01121	CB1-4-2001J	1	
R1.0	RESISTOR,FXD,COMPOSITION,2400OHMS, 1/2W,PORM 5 PCT	905000242	01121	EB1-2-242J	1	
R1.1	RESISTOR,FXD,COMPOSITION,2400OHMS, 1/2W,PORM 5 PCT	905000242	01121	EB1-2-242J	1	
R2.0	RESISTOR,FXD,FILM,4220HMS,1/8W,PORM 1 PCT,METAL FILM	907300070	16299	MA55	1	
R2.1	RESISTOR,FXD,FILM,4220HMS,1/8W,PORM 1 PCT,METAL FILM	907300070	16299	MA55	1	
R3.0	RESISTOR,FXD,FILM,1000OHMS,1/8W,PORM 1 PCT,METAL FILM	907300073	16299	MA55	1	
R3.1	RESISTOR,FXD,FILM,1000OHMS,1/8W,PORM 1 PCT,METAL FILM	907300073	16299	MA55	1	
R4.0	RESISTOR,FXD,FILM,1.62KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300078	16299	MA55	1	
R4.1	RESISTOR,FXD,FILM,1.62KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300078	16299	MA55	1	
R5.0	RESISTOR,FXD,FILM,30.1KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300110	16299	MA55	1	
R5.1	RESISTOR,FXD,FILM,30.1KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300110	16299	MA55	1	
R6.0	RESISTOR,FXD,FILM,121KOHMS,1/4W,PORM 1 PCT, METAL FILM	908310022	16299	MA60	1	
R6.1	RESISTOR,FXD,FILM,121KOHMS,1/4W,PORM 1 PCT, METAL FILM	908310022	16299	MA60	1	
R7.0	RESISTOR,FXD,FILM,12.1KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300102	16299	MA55	1	
R7.1	RESISTOR,FXD,FILM,12.1KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300102	16299	MA55	1	
R8.0	RESISTOR,FXD,FILM,2.15KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300080	16299	MA55	1	
R8.1	RESISTOR,FXD,FILM,2.15KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300080	16299	MA55	1	
R21.2	RESISTOR,FXD,COMPOSITION,10KOHMS,1/2W, PORM 5 PCT	905010103	01121	EB1-2-1002J	1	
R21.3	RESISTOR,FXD,COMPOSITION,10KOHMS,1/2W, PORM 5 PCT	905010103	01121	EB1-2-1002J	1	
R22.2	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PORM 5 PCT	906910682	01121	CB1-4-6801J	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R22.3	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PORM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R23.2	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R23.3	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
	CP3 PRINTED CIRCUIT BOARD ASSEMBLY	D0264860C	94668	C02648600		
	PRINTED CURCUIT BOARD	904500404	94668	904500404	1	
C1	CAPACITOR,FXD,ELECTROLYTIC,100MFD,6V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902710107	56289	150D107X9006R2	1	
C2	CAPACITOR,FXD,ELECTROLYTIC,1MFD,10V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720105	56289	150D105X9010A2	1	
C3	CAPACITOR,FXD,MICA,200PF,300V,PORM 5 PCT,	901900201	93790	CD7FC201J03	1	
CR1					1	
CR2					1	
CR3					1	
CR4					1	
CR5					1	
CR6					1	
IC2-1	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC2-2	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC2-3	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC2-4	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC3-1	INTEGRATED CIRCUIT	920300065	07263	U6A993259X	1	
IC5-1	INTEGRATED CIRCUIT	920300067	07263	U6A994559X	1	
IC6-1	INTEGRATED CIRCUIT	920300064	07263	U6A909759X	1	
IC6-2	INTEGRATED CIRCUIT	920300064	07263	U6A909759X	1	
IC6-3	INTEGRATED CIRCUIT	920300064	07263	U6A909759X	1	
IC6-4	INTEGRATED CIRCUIT	920300064	07263	U6A909759X	1	
IC1-1	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC1-2	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC1-3	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
R1	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R2	RESISTOR,FXD,COMPOSITION,100OHMS,2W, PORM 5 PCT	905800101	C1121	HB-101-5	1	
R3	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	C1121	CB1-4-1002J	1	
R4	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R5	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	C1121	CB1-4-1002J	1	
R6	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R7	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	C1121	CB1-4-1002J	1	
R8	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	C1121	CB1-4-1002J	1	
	CP4 PRINTED CIRCUIT BOARD ASSEMBLY	D0264870D	94668	C02648700		
	PRINTED CURCUIT BOARD	904500405	94668	904500405	1	
C1	CAPACITOR,FXD,ELECTROLYTIC,2.2MFD,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902700225	56289	150D225X9020A2	1	
C2	CAPACITOR,FXD,ELECTROLYTIC,12MFD,20V, PORM 10 PCT, SOLID TANTALUM,SLEEVED	902700126	56289	150D126X9020B2	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
C3	CAPACITOR,FXD,GLASS,C.0056MFD,5CV,PCRM 10 PCT	902900562	16299	CYK01BT562K	1	
C4	CAPACITOR,FXD,GLASS,C.0056MFD,5CV,PCRM 10 PCT	902900562	16299	CYK01BT562K	1	
C5	CAPACITOR,FXD,ELECTROLYTIC,3.3MFD,20V, PORM 10 PCT,SOLID TANTALUM,SLEEVED	902710335	56289	150D335X9020B2	1	
C6	CAPACITOR,FXD,ELECTROLYTIC,3.3MFD,20V, PORM 10 PCT,SOLID TANTALUM,SLEEVED	902710335	56289	150D335X9020B2	1	
C7	CAPACITOR,FXD,ELECTROLYTIC,1MFD,10V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720105	56289	150D105X9010A2	1	
C8	CAPACITOR,FXD,ELECTROLYTIC, 1UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C9	CAPACITOR,FXD,ELECTROLYTIC, 1UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
CR1	DIODE	910500101	12065	1N3666	1	
CR2	DIODE	910500103	07263	1N914	1	
CR3					1	
CR4	DIODE	910500101	12065	1N3666	1	
CR5	DIODE	910500101	12065	1N3666	1	
CR6					1	
CR7	DIODE	910500098	04713	1N816	1	
CR8	DIODE	910500098	04713	1N816	1	
CR9					1	
CR10	DIODE	910500101	12065	1N3666	1	
CR11	DIODE	910500101	12065	1N3666	1	
CR12	DIODE	910500098	04713	1N816	1	
CR13	DIODE	910500098	04713	1N816	1	
CR14	DIODE	910500101	12065	1N3666	1	
CR15					1	
CR16					1	
CR17	DIODE	910500099	07263	1N748A	1	
CR18	DIODE	910500101	12065	1N3666	1	
CR19	DIODE	910500099	07263	1N748A	1	
CR20	DIODE	910500101	12065	1N3666	1	
CR21	DIODE	910500100	07263	1N4610	1	
CR22	DIODE	910500100	07263	1N4610	1	
CR23					1	
CR24					1	
CR25	DIODE	910500103	07263	1N914	1	
CR26	DIODE	910500103	07263	1N914	1	
CR27	DIODE	910500101	12065	1N3666	1	
CR28	DIODE	910500103	07263	1N914	1	
CR29	DIODE	910500103	07263	1N914	1	
CR30	DIODE	910500103	07263	1N914	1	
CR31	DIODE	910500103	07263	1N914	1	
CR32	DIODE	910500101	12065	1N3666	1	
IC1-1	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC1-2	INTEGRATED CIRCUIT	920300069	07263	U6A994659X	1	
IC2-1	INTEGRATED CIRCUIT	920300068	07263	U6A996259X	1	
IC5-1	INTEGRATED CIRCUIT	920300067	07263	U6A994559X	1	
IC7-1	INTEGRATED CIRCUIT	920300063	07263	U6A909459X	1	
IC7-2	INTEGRATED CIRCUIT	920300063	07263	U6A909459X	1	
Q1	TRANSISTOR	910300089	04713	2N956	1	
Q2	TRANSISTOR	910300089	04713	2N956	1	
Q3	TRANSISTOR	910300090	04713	2N718	1	
Q4	TRANSISTOR	910300090	04713	2N718	1	
Q5	TRANSISTOR	910300090	04713	2N718	1	
Q6	TRANSISTOR	910300092	04713	2N527	1	
Q7	TRANSISTOR	910300089	04713	2N956	1	
Q8	TRANSISTOR	910300089	04713	2N956	1	
Q9	TRANSISTOR	910300089	04713	2N956	1	
Q10	TRANSISTOR	910300090	04713	2N718	1	
Q11	TRANSISTOR	910300090	04713	2N718	1	
R1	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R2	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R3	RESISTOR,FXD,COMPOSITION,2000OHMS,1/4W, PORM 5 PCT	906910202	01121	CB1-4-2001J	1	
R4	RESISTOR,FXD,COMPOSITION,3600OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R6	RESISTOR,FXD,COMPOSITION,2000OHMS,1/4W, PORM 5 PCT	906910202	01121	CB1-4-2001J	1	
R7	RESISTOR,FXD,FILM,2610OHMS,PORM 1 PCT,1/8W, PRECISION METAL FILM	907300035	91637	MFF-2611F	1	
R8	RESISTOR,FXD,FILM,4.22KOHMS,1/8W, PORM 1 PCT,METAL FILM	907310036	16299	MA55	1	
R9	RESISTOR,FXD,COMPOSITION,510OHMS,1/4W, PORM 5 PCT	906900511	01121	CB1-4-511J	1	
R10	RESISTOR,FXD,COMPOSITION,510OHMS,1/4W, PORM 5 PCT	906900511	01121	CB1-4-511J	1	
R11	RESISTOR,FXD,COMPOSITION,3600OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R12	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R13	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
R14	RESISTOR,FXD,COMPOSITION,2000OHMS,1/4W, PORM 5 PCT	906910202	01121	CB1-4-2001J	1	
R15	RESISTOR,FXD,COMPOSITION,3600OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R16	RESISTOR,FXD,FILM,1.3KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300075	16299	MA55	1	
R17	RESISTOR,FXD,FILM,7.5KOHMS,1/8W, PORM 1 PCT,METAL FILM	907310039	16299	MA55	1	
R18	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R19	RESISTOR,FXD,COMPOSITION,2000OHMS,1/4W, PORM 5 PCT	906910202	01121	CB1-4-2001J	1	
R20	RESISTOR,FXD,COMPOSITION,1600 OHMS,1/4W, PORM 5 PCT	906900162	01121	CB1-4-1601J	1	
R21	RESISTOR,FXD,COMPOSITION,240OHMS,1/2W, PORM 5 PCT	905010241	01121	EB1-2-241J	1	
R22	RESISTOR,FXD,COMPOSITION,24KOHMS,1/4W, PORM 5 PCT	906900243	01121	CB1-4-2402J	1	
R23	RESISTOR,FXD,COMPOSITION,1000OHMS,1/4W, PORM 5 PCT	906910102	01121	CB1-4-1001J	1	
R24	RESISTOR,FXD,COMPOSITION,1.5KOHMS,1/4W, PORM 5 PCT	906910152	01121	CB1-4-1501J	1	
R25	RESISTOR,FXD,COMPOSITION,270OHMS,1/2W, PORM 5 PCT	905010271	01121	EB1-2-271J	1	
R26	RESISTOR,FXD,COMPOSITION,270OHMS,1/2W, PORM 5 PCT	905010271	01121	EB1-2-271J	1	
R27	RESISTOR,FXD,COMPOSITION,200OHMS,1/2W, PORM 5 PCT	905000201	01121	EB1-2-201J	1	
R28	RESISTOR,FXD,FILM,120KOHMS,1/8W,PORM 1 PCT,METAL FILM	907300117	16299	MA55	1	
R29	RESISTOR,FXD,FILM,825KOHMS,1/8W,PORM 1 PCT,METAL FILM	908300140	16299	MA60	1	
R30	RESISTOR,FXD,COMPOSITION,3600OHMS,1/4W, PORM 5 PCT	906900362	01121	CB1-4-3602J	1	
R31	RESISTOR,FXD,COMPOSITION,2.7KOHMS,1/4W, PORM 5 PCT	906910272	01121	CB1-4-2701J	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	CP5 ASSEMBLY	C02648800	94668	C02648800		
	PRINTED CURCUIT BOARD	904500406	94668	904500406	1	
C1	CAPACITOR,FXD,ELECTROLYTIC,47MFD,15V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902730476	56289	150D476X9015R2	1	
C2	CAPACITOR,FXD,MYLAR,C.22MFD,2CCV, PCRM 1PCT	901120224	56289	420P122	1	
C3	CAPACITOR,FXD,MICA,47CPF,100V,PORM 5 PCT	901910471	93790	CD7FA471J03	1	
C4	CAPACITOR,FXD,MICA,47CPF,1CCV,PORM 5 PCT	901910471	93790	CD7FA471J03	1	
C5	CAPACITOR,FXD,MICA,47CPF,10CV,PORM 5 PCT	901910471	93790	CD7FA471J03	1	
C6	CAPACITOR,FXD,MICA,47CPF,10CV,PORM 5 PCT	901910471	93790	CD7FA471J03	1	
C7	CAPACITOR,FXD,MYLAR,C.027MFD,2CCV,PCRM 1 PCT	901100273	56289	420P127	1	
C8	CAPACITOR,FXD,ELECTROLYTIC, 1UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C9	CAPACITOR,FXD,ELECTRCLYTIC, 1UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
CR1	DIODE	910500101	12065	1N3666	1	
CR2	DIODE	910500101	12065	1N3666	1	
CR3	DIODE	910500101	12065	1N3666	1	
CR4	DIODE	910500101	12065	1N3666	1	
CR5	DIODE	910500101	12065	1N3666	1	
CR6	DIODE	910500101	12065	1N3666	1	
CR7	DIODE	910500101	12065	1N3666	1	
CR8	DIODE	910500101	12065	1N3666	1	
CR9	DIODE	910500101	12065	1N3666	1	
CR10	DIODE	910500101	12065	1N3666	1	
CR11	DIODE	910500101	12065	1N3666	1	
CR12	DIODE	910500101	12065	1N3666	1	
CR13	DIODE	910500101	12065	1N3666	1	
CR14	DIODE	910500101	12065	1N3666	1	
CR15	DIODE	910500101	12065	1N3666	1	
CR16	DIODE	910500101	12065	1N3666	1	
CR17	DIODE	910500101	12065	1N3666	1	
CR18	DIODE	910500101	12065	1N3666	1	
CR19	DIODE	910500101	12065	1N3666	1	
CR20	DIODE	910500101	12065	1N3666	1	
CR21	DIODE	910500103	07263	1N914	1	
CR22	DIODE	910500103	07263	1N914	1	
CR23	DIODE	910500102	07263	1N753A	1	
CR24	DIODE	910500103	07263	1N914	1	
CR25	DIODE	910500101	12065	1N3666	1	
CR26	DIODE	910500102	07263	1N753A	1	
CR27	DIODE	910500101	12065	1N3666	1	
CR28	DIODE	910500103	07263	1N914	1	
CR29	DIODE	910500101	12065	1N3666	1	
CR30	DIODE	910500103	07263	1N914	1	
CR31	DIODE	910500098	04713	1N816	1	
CR32	DIODE	910500101	12065	1N3666	1	
CR33	DIODE	910500101	12065	1N3666	1	
CR34	DIODE	910500101	12065	1N3666	1	
CR35	DIODE	910500101	12065	1N3666	1	
CR37	DIODE	910500101	12065	1N3666	1	
CR38	DIODE	910500101	12065	1N3666	1	
Q1	TRANSISTOR	910300090	04713	2N718	1	
Q2	TRANSISTOR	910300090	04713	2N718	1	
Q3	TRANSISTOR	910300091	04713	2N3250	1	
Q4	TRANSISTOR	910300089	04713	2N956	1	
Q5	TRANSISTOR	910300089	04713	2N956	1	
Q6	TRANSISTOR	910300090	04713	2N718	1	
Q7	TRANSISTOR	910300090	04713	2N718	1	
Q8	TRANSISTOR	910300090	04713	2N718	1	
Q9	TRANSISTOR	910300090	04713	2N718	1	
Q10	TRANSISTOR	910300089	04713	2N956	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
Q11	TRANSISTOR	910300090	04713	2N718	1	
R1	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R2	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R3	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	01121	CB1-4-6801J	1	
R4	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R5	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	01121	CB1-4-6801J	1	
R6	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R7	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R8	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R9	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PERM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R10	RESISTOR,FXD,FILM,10KOHMS,1/8W,PERM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R11	RESISTOR,FXD,COMPOSITION,27KOHMS, 1/4W,PERM 5 PCT	906910273	C1121	CB1-4-2702J	1	
R12	RESISTOR,FXD,FILM,10KOHMS,1/8W,PERM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R13	RESISTOR,FXD,FILM,51.1KOHMS,1/8W,PERM 1 PCT METAL FILM	907300114	16299	MA55	1	
R14	RESISTOR,FXD,FILM,51.1KOHMS,1/8W,PERM 1 PCT METAL FILM	907300114	16299	MA55	1	
R15	RESISTOR,FXD,FILM,30100OHMS,1/8W, PERM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R16	RESISTOR,FXD,COMPOSITION,4.3KOHMS,1/4W, PERM 5 PCT	906900432	01121	CB1-4-4301J	1	
R17	RESISTOR,FXD,FILM,77.7KOHMS,1/8W,PERM 1/2 PCT,METAL FILM	907300116	16299	MA55	1	
R18	RESISTOR,FXD,FILM,76.8KOHMS,1/8W,PERM 1 PCT,METAL FILM	907300115	16299	MA55	1	
R19	RESISTOR,FXD,COMPOSITION,4.3KOHMS,1/4W, PERM 5 PCT	906900432	01121	CB1-4-4301J	1	
R20	RESISTOR,FXD,FILM,30100OHMS,1/8W, PERM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R21	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R22	RESISTOR,FXD,FILM,30.1KOHMS,1/8W,PERM 1 PCT,METAL FILM	907300110	16299	MA55	1	
R23	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R24	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R25	RESISTOR,FXD,FILM,30100HMS,1/8W, PERM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R26	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R27	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R28	RESISTOR,FXD,FILM,30100HMS,1/8W, PERM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R29	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R30	RESISTOR,FXD,FILM,20KOHMS,1/8W,PERM 1 PCT,METAL FILM	907300107	16299	MA55	1	
R31	RESISTOR,FXD,FILM,15000OHMS,1/8W,PERM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R32	RESISTOR,FXD,FILM,30100OHMS,1/8W, PERM 1 PCT,METAL FILM	907300081	16299	MA55	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R33	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R34	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R35	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R36	RESISTOR,FXD,FILM,15COCCHMS,1/8W,PORM 1 PCT,METAL FILM	907300104	16299	MA55	1	
R37	RESISTOR,FXD,COMPOSITION,10KOHMS,1/4W, PORM 5 PCT	906910103	01121	CB1-4-1002J	1	
	CP8 ASSEMBLY	D02648900	94668	D02648900		
	PRINTED CURCUIT BOARD	904500407	94668	904500407	1	
C3	CAPACITOR,FXD,ELECTROLYTIC, 1UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C4	CAPACITOR,FXD,ELECTROLYTIC, 1UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C1.0	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.1	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.2	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.3	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.4	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.5	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.6	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.7	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C1.8	CAPACITOR,FXD,MICA,27CPF,30CV,PORM 5 PCT	901910271	93790	CD7FC271J03	1	
C2.9	CAPACITOR,FXD,GLASS,C.C15MFD,5CV, PORM 10 PCT, AXIAL LEAD	902900153	16299	CYK02BT153K	1	
C2.10	CAPACITOR,FXD,GLASS,C.015MFD,5CV, PORM 10 PCT, AXIAL LEAD	902900153	16299	CYK02BT153K	1	
CR1.9	DIODE	910500101	12065	1N3666	1	
CR2.9	DIODE	910500101	12065	1N3666	1	
CR3.9	DIODE	910500103	07263	1N914	1	
CR1.10	DIODE	910500101	12065	1N3666	1	
CR2.10	DIODE	910500101	12065	1N3666	1	
CR3.10	DIODE	910500103	07263	1N914	1	
CR4.11	DIODE	910500101	12065	1N3666	1	
CR4.12	DIODE	910500101	12065	1N3666	1	
CR4.13	DIODE	910500101	12065	1N3666	1	
CR4.14	DIODE	910500101	12065	1N3666	1	
CR4.15	DIODE	910500101	12065	1N3666	1	
CR4.16	DIODE	910500101	12065	1N3666	1	
CR4.17	DIODE	910500101	12065	1N3666	1	
CR4.18	DIODE	910500101	12065	1N3666	1	
Q1.0	TRANSISTOR	910300090	04713	2N718	1	
Q1.1	TRANSISTOR	910300090	04713	2N718	1	
Q1.2	TRANSISTOR	910300090	04713	2N718	1	
Q1.3	TRANSISTOR	910300090	04713	2N718	1	
Q1.4	TRANSISTOR	910300090	04713	2N718	1	
Q1.5	TRANSISTOR	910300090	04713	2N718	1	
Q1.6	TRANSISTOR	910300090	04713	2N718	1	
Q1.7	TRANSISTOR	910300090	04713	2N718	1	
Q1.8	TRANSISTOR	910300090	04713	2N718	1	
Q2.9	TRANSISTOR	910300092	04713	2N527	1	
Q2.10	TRANSISTOR	910300092	04713	2N527	1	
Q4.11	TRANSISTOR	910300089	04713	2N956	1	
Q4.12	TRANSISTOR	910300089	04713	2N956	1	
Q4.13	TRANSISTOR	910300089	04713	2N956	1	
Q4.14	TRANSISTOR	910300089	04713	2N956	1	
Q4.15	TRANSISTOR	910300089	04713	2N956	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
C4.16	TRANSISTOR	910300089	C4713	2N956	1	
C4.17	TRANSISTOR	910300089	C4713	2N956	1	
C4.18	TRANSISTOR	910300089	C4713	2N956	1	
R9	RESISTOR,FXD,COMPOSITION,6.8KOHMS,1/4W, PORM 5 PCT	906910682	C1121	CB1-4-6801J	1	
R1.0	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R1.1	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R1.2	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	C1121	CB1-4-5101J	1	
R1.3	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	C1121	CB1-4-5101J	1	
R1.4	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R1.5	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	C1121	CB1-4-5101J	1	
R1.6	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	01121	CB1-4-5101J	1	
R1.7	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	C1121	CB1-4-5101J	1	
R1.8	RESISTOR,FXD,COMPOSITION,5.1KOHMS,1/4W, PORM 5 PCT	906910512	C1121	CB1-4-5101J	1	
R2.0	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.1	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.2	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.3	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R2.4	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.5	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.6	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R2.7	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R2.8	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	C1121		1	
R3.9	RESISTOR,FXD,FILM,10CKOHMS,1/8W, PORM 1 PCT,METAL FILM	907310043	16299	MA55	1	
R4.9	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R5.9	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R6.9	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R7.9	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R3.10	RESISTOR,FXD,FILM,10CKOHMS,1/8W, PORM 1 PCT,METAL FILM	907310043	16299	MA55	1	
R4.10	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R5.10	RESISTOR,FXD,FILM,30100HMS,1/8W, PORM 1 PCT,METAL FILM	907300081	16299	MA55	1	
R6.10	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R7.10	RESISTOR,FXD,FILM,10KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300100	16299	MA55-1002F	1	
R8.11	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.12	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	C1121	CB1-4-3001J	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R8.13	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.14	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.15	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.16	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.17	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R8.18	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
	PANEL ASSEMBLY	C02807501	94668	C02807501		
	DISPLAY SHIELD	C02807700	94668	C02807700	1	
	PANEL ASSEMBLY	C02806701	94668	C02806701	1	
	METER,WESTON	911800124	65092	260752	1	
	SPEAKER	921400003	28869	15003P1WAK2-1A	1	
CP9	CP9 ASSEMBLY	C02649000	94668	C02649000	1	
CP10	CP10 ASSEMBLY	C02649901	94668	C02649901	1	
CP11	CP11 ASSEMBLY	C02650001	94668	C02650001	1	
CP12	CP12 ASSEMBLY	C02650101	94668	C02650101	1	
CP14	CP14 CIRCUIT PACK ASSEMBLY	C02649500	94668	C02649500	1	
	CP9 ASSEMBLY	C02649000	94668	C02649000		
	PRINTED CIRCUIT BOARD	904500368	94668	904500368	1	
	SOCKET,NIXIE	914000054	16770	SK144	2	
C1	CAPACITOR,FXD,GLASS,0.0022MFD,5CV, PORM 10 PCT, AXIAL LEAD	902900222	16299	CYK01BT222K	1	
C2	CAPACITOR,FXD,GLASS,0.01MFD,5CV,PORM 10 PCT,AXIAL LEAD	902900103	16299	CYK01BT103K	1	
C3	CAPACITOR,FXD,ELECTROLYTIC,1MFD,10V, PORM 10 PCT,SOLID TANTALUM, SLEEVED	902720105	56289	150D1C5X9010A2	1	
CR1	DIODE	910500103	07263	1N914	1	
CR2	DIODE	910500103	07263	1N914	1	
IC8-1	INTEGRATED CIRCUIT	920300071	07263	U6A995879X	1	
IC8-2	INTEGRATED CIRCUIT	920300071	07263	U6A995879X	1	
IC9-1	INTEGRATED CIRCUIT	920300072	07263	U6B996079X	1	
IC9-2	INTEGRATED CIRCUIT	920300072	07263	U6B996079X	1	
Q1	TRANSISTOR	910300090	04713	2N718	1	
Q2	TRANSISTOR	910300090	04713	2N718	1	
Q3	TRANSISTOR	910300090	04713	2N718	1	
Q4	TRANSISTOR	910300090	04713	2N718	1	
Q5	TRANSISTOR	910300089	04713	2N956	1	
R2	RESISTOR,FXD,COMPOSITION,510CHMS,1/4W, PORM 5 PCT	906900511	01121	CB1-4-511J	1	
R3	RESISTOR,FXD,COMPOSITION,8.2KOHMS, 1/4W, PORM 5 PCT	906910822	01121	CB1-4-8201J	1	
R4	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R5	RESISTOR,FXD,COMPOSITION,510CHMS,1/4W, PORM 5 PCT	906900511	01121	CB1-4-511J	1	
R6	RESISTOR,FXD,COMPOSITION,30CCOHMS,1/4W, PORM 5 PCT	906910302	01121	CB1-4-3001J	1	
R7	RESISTOR,FXD,COMPOSITION,3.3KOHMS, 1/4W,PORM 5 PCT	906910332	01121	CB1-4-3301J	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R8	RESISTOR,FXD,COMPOSITION,51CCHMS,1/4W, PORM 5 PCT	906900511	C1121	CB1-4-511J	1	
R9	RESISTOR,FXD,COMPOSITION,4.7KCHMS,1/4W, PORM 5 PCT	906910472	C1121	CB1-4-4701J	1	
R10	RESISTOR,FXD,COMPOSITION,4.7KCHMS,1/4W, PORM 5 PCT	906910472	C1121	CB1-4-4701J	1	
R11	RESISTOR,FXD,COMPOSITION,3.3KCHMS, 1/4W,PORM 5 PCT	906910332	01121	CB1-4-3301J	1	
R12	RESISTOR,FXD,COMPOSITION,10CCCHMS,1/4W, PORM 5 PCT	906910102	01121	CB1-4-1001J	1	
R13	RESISTOR,FXD,COMPOSITION,10CCCHMS,1/4W, PORM 5 PCT	906910102	01121	CB1-4-1001J	1	
R1.0	RESISTOR,FXD,COMPOSITION,22KCHMS,1W, PORM 5 PCT	905400223	01121	CB1-2202J	1	
R1.1	RESISTOR,FXD,COMPOSITION,22KOHMS,1W, PORM 5 PCT	905400223	01121	CB1-2202J	1	
V1.0	TUBE,NIXIE,STD RECT	910700113	16770	B-5991	1	
V1.1	TUBE,NIXIE,STD RECT	910700113	16770	B-5991	1	
		C02649501				
	PRINTED CIRCUIT BOARD ASSEMBLY	C02650201	94668	C02650201	1	
C1	CAPACITOR,FXD,MYLAR,24.5MFD,200V,PCRM 1 PCT	901102255	56289	431P122	1	
C2	CAPACITOR,FXD,MYLAR,1.6MFD,200V,PCRM 1 PCT	901100165	56289	420P125	1	
	CP10 ASSEMBLY	C02649901	94668	C02649901		
	CP10 ASSEMBLY PRINTED CIRCUIT	C02649100	94668	C02649100	1	
	CP11 ASSEMBLY	C02650001	94668	C02650001		
	CP11 ASSEMBLY PRINTED CIRCUIT	C02649200	94668	C02649200	1	
	CP12 ASSEMBLY	C02650101	94668	C02650101		
	CP12 BOARD ASSEMBLY	C02649300	94668	C02649300	1	
	CP12 BOARD ASSEMBLY	C02649300	94668	C02649300	1	
	PANEL ASSEMBLY	D02806701	94668	D02806701		
					1	
	PANEL ASSEMBLY	D02806601	94668	D02806601	1	
	POWER PANEL ASSEMBLY	D02806901	94668	D02806901	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	CP10 ASSEMBLY PRINTED CIRCUIT	C02649100	94668	C02649100		
	PRINTED CURCUIT BOARD	904500409	94668	904500409	1	
C1	CAPACITOR,FXD,MYLAR,0.792MFD,200V,PCRM 1PCT	901107923	56289	420P124	1	
C2	CAPACITOR,FXD,MYLAR,0.39MFD,200V,PCRM 1 PCT	901100394	56289	420P123	1	
C3	CAPACITOR,FXD,MYLAR,0.22MFD,200V, PCRM 1PCT	901120224	56289	420P122	1	
C4	CAPACITOR,FXD,MYLAR,0.18MFD,200V,PCRM 1 PCT	901100184	56289	420P121	1	
C5	CAPACITOR,FXD,MYLAR,0.152MFD,200V,PCRM 1 PCT	901101523	56289	420P120	1	
C6	CAPACITOR,FXD,MYLAR,0.13MFD,200V,PCRM 1 PCT	901100134	56289	420P119	1	
C7	CAPACITOR,FXD,MYLAR,0.113MFD,200V,PCRM 1 PCT	901101133	56289	420P118	1	
C8	CAPACITOR,FXD,MYLAR,0.098MFD,200V,PCRM 1 PCT	901100983	56289	420P117	1	
C9	CAPACITOR,FXD,MYLAR,0.0776MFD,200V PCRM 1 PCT	901107762	56289	420P126	1	
C10	CAPACITOR,FXD,MYLAR,2.4MFD,200V,PCRM 1 PCT	901100245	56289	431P121	1	
	CP11 ASSEMBLY PRINTED CIRCUIT	C02649200	94668	C02649200		
	PRINTED CURCUIT BOARD	904500410	94668	904500410	1	
R1	RESISTOR,FXD,FILM,4.59KOHMS,1/8W,PCRM 1/2 PCT,METAL FILM	907300088	16299	NA55	1	
R2	RESISTOR,FXD,FILM,8.66KOHMS,1/8W,PCRM 1 PCT,METAL FILM	907300098	16299	NA55	1	
R3	RESISTOR,FXD,FILM,4.22KOHMS,1/8W, PORM 1 PCT,METAL FILM	907310036	16299	NA55	1	
R4	RESISTOR,FXD,FILM,10.4KOHMS,2/8W,PCRM 1/2 PCT,METAL FILM	907300101	16299	NA55	1	
R5	RESISTOR,FXD,FILM,3.92KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300086	16299	NA55	1	
R6	RESISTOR,FXD,FILM,12.7KOHMS,1/8W,PCRM 1 PCT,METAL FILM	907300103	16299	NA55	1	
R7	RESISTOR,FXD,FILM,3.65KOHMS,1/8W,PCRM 1 PCT,METAL FILM	907300085	16299	NA55	1	
R8	RESISTOR,FXD,FILM,16.7KOHMS,1/8W,PCRM 1/2 PCT,METAL FILM	907300105	16299	NA55	1	
R9	RESISTOR,FXD,FILM,3.44KOHMS,1/8W,PCRM 1/2 PCT,METAL FILM	907300084	16299	NA55	1	
R10	RESISTOR,FXD,FILM,24OHMS,1/8W,PORM 1/2 PCT,METAL FILM	907300109	16299	NA55	1	
R11	RESISTOR,FXD,FILM,5.49KOHMS,1/8W, PORM 1 PCT, METAL FILM	907300092	16299	NA55	1	
R12	RESISTOR,FXD,FILM,6.57KOHMS,1/8W, PORM 1/2 PCT,METAL FILM	907300095	16299	NA55	1	
R13	RESISTOR,FXD,FILM,6.12KOHMS,1/8W, PORM 1/2 PCT,METAL FILM	907300094	16299	NA55	1	
R14	RESISTOR,FXD,FILM,5.9KOHMS,1/8W, PORM 1 PCT, METAL FILM	907300093	16299	NA55	1	
R15	RESISTOR,FXD,FILM,6.9KOHMS,1/7W, PORM 1/2 PCT,METAL FILM	907300096	16299	NA55	1	
R16	RESISTOR,FXD,FILM,5.3KOHMS,1/8W, PORM 1/2 PCT,METAL FILM	907300091	16299	NA55	1	
R17	RESISTOR,FXD,FILM,7.87KOHMS,1/8W,PCRM 1 PCT METAL FILM	907300097	16299	NA55	1	
R18	RESISTOR,FXD,FILM,4.81KOHMS,1/8W, PORM 1/2 PCT,METAL FILM	907300089	16299	NA55	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R19	RESISTOR,FXD,FILM,9.2KOHMS,1/8W,PCRM 1/2 PCT,METAL FILM	907300099	16299	MA55	1	
R20	RESISTOR,FXD,FILM,4.42KOHMS,1/8W, PORM 1 PCT,METAL FILM	907300087	16299	MA55	1	
R21	RESISTOR,FXD,WW,14.1 OHMS,0.1W,PORM 1 PCT	906100168	17870	1402	1	
R22	RESISTOR,FXD,WW,28.2OHMS,0.1W,PORM 1 PCT	906100169	17870	1402	1	
R23	RESISTOR,FXD,WW,56.4OHMS,0.1W,PORM 1 PCT	906100170	17870	1402	1	
R24	RESISTOR,FXD,WW,112.8OHMS,0.1W,PORM 1PCT	906100173	17870	1402	1	
R25	RESISTOR,FXD,WW,147OHMS,1/8W,PORM 1 PCT	906100174	17870	1403	1	
R26	RESISTOR,FXD,WW,11500HMS,0.1W,PORM 1 PCT	906110176	17870	1402	1	
R27	RESISTOR,FXD,WW,2100HMS,0.1W,PORM 1 PCT	906100175	17870	1402	1	
R28	RESISTOR,FXD,WW,1100HMS,0.1W,PORM 1 PCT	906100172	17870	1402	1	
R29	RESISTOR,FXD,WW,1010HMS,0.1W,PORM 1 PCT	906100171	17870	1402	1	
R30	RESISTOR,FXD,COMPOSITION,100OHMS, 1/2W, PORM 5 PCT	905000101	01121	EB1-2-101J	1	
R31	RESISTOR,FXD,COMPOSITION,200OHMS,1/2W, PORM 5 PCT	905000201	01121	EB1-2-201J	1	
R32	RESISTOR,FXD,COMPOSITION,180OHMS,1/2W, PORM 5 PCT	905010181	01121	EB1-2-181J	1	
R33	RESISTOR,FXD,COMPOSITION,2.4KOHMS,1/4W, PORM 5 PCT	906910242	01121	CB1-4-2401J	1	
R34	RESISTOR,FXD,COMPOSITION,200OHMS,1/2W, PORM 5 PCT	905000201	01121	EB1-2-201J	1	
R35	RESISTOR,VARIABLE,25OOHMS,PORM 10 PCT	907900324	01121	FR251U	1	
	CP12 BOARD ASSEMBLY	C02649300	94668	C02649300		
	PRINTED CIRCUIT BOARD	B02810701	94668	B02810701	1	
	HEAT SINK	921300006	13103	2218B	1	
C1	CAPACITOR,FXD,MYLAR,2.5MFD,2OOV, PCRM 10 PCT	901100255	56289	430P25592	1	
C2	CAPACITOR,FXD,ELECTROLYTIC,0.22MFD,6V, PORM 10 PCT, SOLID TANTALUM,SLEEVED	902700224	56289	150D224X9006A2	1	
C3	CAPACITOR,FXD,ELECTROLYTIC,1MFD,6V,PCRM 10 PCT, SOLID TANTALUM,SLEEVED	902710105	56289	150D1C5X9006A2	1	
C4	CAPACITOR,FXD,MICA,100PF,300V,PORM 5 PCT	901920101	93790	CD6FC101J03	1	
C5	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C6	CAPACITOR,FXD,CERAMIC,0.022MFD,25V, PORM 20 PCT,RADIAL LEADS	901400223	56289	3C023223X025DA	1	
C7	CAPACITOR,FXD,MICA,10PF,500V,PCRM 10 PCT	901910100	93790	CD6CD100K03	1	
C8	CAPACITOR,FXD,ELECTROLYTIC,600OMFD,6V,PCRM 75 PCT,AXIAL LEADS	902200608	56289	39D608G006HP0	1	
C9	CAPACITOR,FXD,ELECTROLYTIC,330MFD,6V, PORM 10PCT,SOLID TANTALUM,SLEEVED	902710337	56289	150D337X9006S2	1	
C10	CAPACITOR,FXD,ELECTROLYTIC,100MFD,6V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902710107	56289	150D1C7X9006R2	1	
C11	CAPACITOR,FXD,ELECTROLYTIC,100MFD,6V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902710107	56289	150D1C7X9006R2	1	
C12	CAPACITOR,FXD,ELECTROLYTIC,6.8MFD,6V, PORM 10 PCT,SOLID TANTALUM,SLEEVED	902700685	56289	150D685X9006A2	1	
C13	CAPACITOR,FXD,GLASS,0.01MFD,5OV,PCRM 10 PCT,AXIAL LEAD	902900103	16299	CYK01BT103K	1	
C14	CAPACITOR,FXD,ELECTROLYTIC, 1UF,2OV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902740105	56289	150D105X9020A2	1	
C15	CAPACITOR,FXD,ELECTROLYTIC, 22UF,20V, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902710226	56289	150D226X9020R2	1	
CR1	DIODE	910500100	07263	1N4610	1	
CR2	DIODE	910500100	07263	1N4610	1	
CR3	DIODE	910500100	07263	1N4610	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
CR4	CIODE	910500098	C4713	1N816	1	
CR5	CIODE	910500098	04713	1N816	1	
CR6	TRANSISTOR	910500092	73293	1N695	1	
CR7	TRANSISTOR	910500092	73293	1N695	1	
IC10-1	INTEGRATED CIRCUIT	920300062	07263	U5B770939X	1	
Q1	TRANSISTOR	910300089	C4713	2N956	1	
R1	RESISTOR,FXD,WW, 17.6K CHMS,C.1W, PORM 1 PCT	906100178	17870	1402	1	
R2	RESISTOR,FXD,WW,60.85KOHMS,1/8W,PORM 1 PCT	906100165	17870	1274	1	
R3	RESISTOR,FXD,WW,136.8KOHMS,C.1W, PORM 1 PCT	906100179	17870	1402	1	
R4	RESISTOR,FXD,WW,432.5KOHMS,1/8W, PORM 1 PCT	906100166	17870	1274	1	
R5	RESISTOR,FXD,WW,89.8OHMS,0.1W, PORM 1 PCT	906100182	17870	1402	1	
R6	RESISTOR,FXD,COMPOSITION,36OHMS,1/2W, PORM 5 PCT	905010560	C1121	EB1-2-360J	1	
R7	RESISTOR,FXD,FILM,511OHMS,1/4W,PORM 1 PCT,METAL FILM	908300108	16299	MA6C	1	
R8	RESISTOR,FXD,COMPOSITION,10KOHMS,1/2W, PORM 5 PCT	905010103	01121	EB1-2-1002J	1	
R9	RESISTOR,FXD,FILM,51.1KOHMS,1/8W,PORM 1 PCT METAL FILM	907300114	16299	MA55	1	
R10	RESISTOR,FXD,FILM,51.1KOHMS,1/8W,PORM 1 PCT METAL FILM	907300114	16299	MA55	1	
R11	RESISTOR,FXD,FILM,2CCOOHMS,1/8W, PORM 1 PCT,METAL FILM	907300079	16299	MA55	1	
R12	RESISTOR,FXD,FILM,1.5KOHMS,1/8W,PORM 1 PCT, METAL FILM	907300077	16299	MA55	1	
R13	RESISTOR,FXD,WW,5.52OHMS,C.1W,PORM 1 PCT	906100167	17870	1402	1	
R14	RESISTOR,FXD,FILM,10CKOHMS,1/8W, PORM 1 PCT,METAL FILM	907310043	16299	MA55	1	
R15	RESISTOR,FXD,FILM,10CKOHMS,1/8W, PORM 1 PCT,METAL FILM	907310043	16299	MA55	1	
R16	RESISTOR,FXD,FILM,237OHMS,1/8W, PORM 1 PCT, METAL FILM	907300068	16299	MA55	1	
R17	RESISTOR,VARIABLE,10COHM,PORM 10 PCT	907900306	C1121	GWBL	1	
R18	RESISTOR,FXD,COMPOSITION,3.6KOHMS, 1/2W,PORM 5 PCT	905000362	01121	EB1-2-3601J	1	
R19	RESISTOR,FXD,COMPOSITION, 4.3KOHMS, 1/2W, PORM 5 PCT	905000432	C1121	EB1-2-4301J	1	
R20	RESISTOR,FXD,COMPOSITION,47OHMS, 1/2W,PORM 5 PCT	905010470	C1121	EB1-2-470J	1	
R21	RESISTOR,FXD,COMPOSITION,3CCOHMS,1/2W, PORM 5 PCT	905000301	C1121	EB1-2-301J	1	
R22	RESISTOR,FXD,WW,9.31KOHMS,C.1W,PORM 1 PCT	906100177	17870	1402	1	
R23	RESISTOR,FXD,FILM,20KOHMS,1/2W,PORM 1 PCT, METAL FILM	908300112	16299	MA65	1	
T1	TRANSFORMER	910000114	00348	M6217	1	
T2	TRANSFORMER	910000115	00348	M6218	1	
	PANEL ASSEMBLY	D02806601	94668	D02806601		
	PANEL ASSEMBLY	D02806401	94668	D02806401	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	POWER PANEL ASSEMBLY	D02806901	94668	C02806901		
	POWER PANEL	C02809301	94668	C02809301	1	
	PANEL ASSEMBLY	C02806401	94668	C02806401		
	TERMINAL BOARD ASSEMBLY	C02337600	94668	C02337600	1	
	PANEL ASSEMBLY	C02806101	94668	D02806101	1	
	POWER PANEL	D02809301	94668	C02809301		
	PANEL POWER	D02809400	94668	C02809400	1	
	CAPACITOR,FXD,ELECTROLYTIC,23CCMFD,	902200238	56289	32D232G020AA6C	1	
	CAPACITOR,FXD,ELECTROLYTIC,3CCCMFD	902200308	56289	32D302G030AB6C	1	
	CAPACITOR,FXD,ELECTROLYTIC,46CC MFD,	902200468	56289	32D462G030AC6C	1	
	TRANSFORMER,	910000113	08779	5604A	1	
	TRANSISTOR	910300087	04713	2N1539A	3	
	FUSE,1/2AMP,250V	913200039	71400	MCL1-2AMP,250V	2	
	FUSE,6/10AMP,250V	913200043	71400	AGC6-10AMP,250	2	
	FUSE,1/2AMP,250V	913200044	71400	AGC1-2AMP,250V	2	
	FUSE,3/4AMP,250V	913200045	71400	AGC3-4AMP,250V	2	
	FUSE,3/8AMP,250V	913200046	71400	AGC3-8AMP,250V	2	
	FUSEHOLDER,FOR 3AG FUSE	913400001	75915	342003	5	
CP13	CP13 ASSEMBLY	D02649401	94668	C02649401	1	
	TERMINAL BOARD ASSEMBLY	C02337600	94668	C02337600		
	TERMINAL BOARD	B02866300	94668	B02866300	1	
R34.0	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.1	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.2	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.3	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.4	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.5	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.6	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
R34.7	RESISTOR,FXD,WW,3000HMS,3W,PCRM 5 PCT	906220301	09746	3X300	1	
	CP13 ASSEMBLY	C02649401	94668	C02649401		
	PRINTED CURCUIT BOARD	904500412	94668	904500412	1	
C1	CAPACITOR,FXD,ELECTROLYTIC,35MFD,3COV, M10 PCT,P50 PCT,AXIAL LEADS	902200356	56289	34D356F300GL2	1	
C2	CAPACITOR,FXD,ELECTROLYTIC, 47UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902720476	56289	150D476X9020R2	1	
C3	CAPACITOR,FXD,ELECTROLYTIC, 47UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902720476	56289	150D476X9020R2	1	
C4	CAPACITOR,FXD,ELECTROLYTIC,1CCMFD,15V,PCRM 10 PCT,SOLID TANTALUM, SLEEVED	902730107	56289	150D1C7X901552	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
C5	CAPACITOR,FXD,ELECTRCLYTIC, 47UF,2CV, PORM 10 PCT, SOLID TANTALUM, SLEEVED	902720476	56289	150D476X9020R2	1	
CR1	CIODE	910500096	C4713	1N4005	1	
CR2	CIODE	910500095	04713	1N4720	1	
CR3	CIODE	910500095	04713	1N4720	1	
CR4	CIODE	910500095	04713	1N4720	1	
CR5	CIODE	910500095	04713	1N4720	1	
CR6	CIODE	910500094	C4713	1N3022B	1	
CR7	CIODE	910500093	04713	1N3829A	1	
CR8	CIODE	910500104	C7263	1N751A	1	
CR9	CIODE	910500094	04713	1N3022B	1	
CR10	CIODE	910500095	04713	1N4720	1	
CR11	CIODE	910500095	C4713	1N4720	1	
Q1	TRANSISTOR	910300089	C4713	2N956	1	
Q2	TRANSISTOR	910300089	C4713	2N956	1	
Q3	TRANSISTOR,SILICON CONTRCLLED RECTIFIER	910300088	C4713	2N4183	1	
R1	RESISTOR,FXD,FILM,10CKOHMS,1W,PORM 2 PCT,METAL FILM	907600015	16299	C32	1	
R2	RESISTOR,FXD,WW,4.7K OHMS,1W, PORM 5 PCT	906200472	C9746	1X	1	
R3	RESISTOR,FXD,WW,4.7K OHMS,1W, PORM 5 PCT	906200472	C9746	1X	1	
R4	RESISTOR,FXD,WW,100HMS,1CW,PCRM 5 PCT	906400100	C9746	10XM	1	
R5	RESISTOR,FXD,WW,200 CHMS,2W, PORM 5 PCT	906200201	C9746	2X	1	
R6	RESISTOR,FXD,WW,47COHMS,1W,PCRM 5 PCT	906210471	09746	1X	1	
R7	RESISTOR,FXD,WW,360 OHMS,1W,PCRM 5 PCT	906200361	09746	1X	1	
R8	RESISTOR,FXD,FILM,301CHMS,1/4W,PORM 1 PCT, METAL FILM	908300107	16299	MA60	1	
R9	RESISTOR,FXD,FILM,1130HMS,1/4W,PORM 1 PCT, METAL FILM	908300104	16299	MA60	1	
R10	RESISTOR,FXD,FILM,10CHMS,1/4W,PORM 1 PCT, METAL FILM	908310076	16299	MA60	1	
R11	RESISTOR,FXD,FILM,20CHMS,1/4W,PORM 1 PCT, METAL FILM	908300102	16299	MA60	1	
R12	RESISTOR,FXD,FILM,40.2OHMS,1/4W,PCRM 1 PCT,METAL FILM	908300103	16299	MA60	1	
R13	RESISTOR,FXD,FILM,576OHMS,1/4W,PORM 1 PCT, METAL FILM	908310025	16299	MA60	1	
R14	RESISTOR,FXD,WW,100HMS,1W,PCRM 5 PCT	906200100	09746	1X	1	
R15	RESISTOR,FXD,WW,10HM,5W,PORM 5 PCT	906220010	C9746	5XM	1	
R16	RESISTOR,FXD,WW,4.7K OHMS,1W, PORM 5 PCT	906200472	09746	1X	1	
R17	RESISTOR,FXD,WW,100HMS,1W,PCRM 5 PCT	906200100	09746	1X	1	
R18	RESISTOR,FXD,WW,680OHMS,1W,PCRM 5 PCT	906200681	09746	1X	1	
R19	RESISTOR,FXD,WW,150HMS,1CW,PCRM 5 PCT	906400150	09746	10XM	1	
R20	RESISTOR,FXD,WW,1KOHMS,1W,PCRM 5 PCT	906210102	09746	1X	1	
R21	RESISTOR,FXD,WW,1KOHMS,1W,PCRM 5 PCT	906210102	09746	1X	1	
R22	RESISTOR,FXD,WW,1KOHMS,1W,PCRM 5 PCT	906210102	09746	1X	1	
R23	RESISTOR,FXD,WW,1KOHMS,1W,PCRM 5 PCT	906210102	09746	1X	1	
	PANEL ASSEMBLY	C02806101	94668	C02806101		
	CABLE ASSEMBLY	B02789201	94668	B02789201	1	
	CABLE ASSEMBLY	B02789202	94668	B02789202	1	
	CABLE ASSEMBLY	B02789300	94668	B02789300	1	
	CP RACK ASSEMBLY	D02805100	94668	D02805100	1	
	PANEL ASSEMBLY	C02805901	94668	C02805901	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	PANEL ASSEMBLY	C02805901	94668	C02805901		
	TERMINAL BOARD ASSEMBLY	C02337600	94668	C02337600	1	
	PANEL ASSEMBLY	C02805501	94668	C02805201	1	
	PANEL ASSEMBLY	D02805501	94668	C02805201		
	TERMINAL BOARD ASSEMBLY	C02337600	94668	C02337600	1	
	PANEL ASSEMBLY	D02805201	94668	C07805201	1	
	PANEL ASSEMBLY	D02805201	94668	C07805201		
	PANEL ASSEMBLY	C02784301	94668	C02784301	1	
	FRONT PANEL ASSEMBLY	D02650401	94668	C02650401		
	PLATE	B02650301	94668	B02650301	1	
	FRONT PANEL	D02647001	94668	C02647001	1	
	RESISTOR,VARIABLE,2 SECTIONS,25COOHMS,500 OHMS,10 PCT LINEAR TAPER	907900302	71590	BAS1209-027	1	
	RESISTOR,VARIABLE,10CCCHMS,PCRM 10 PCT	9C7900303	01121	GW	1	
	RESISTOR,VARIABLE,50COHMS,PORM 10 PCT	907900304	01121	GW	1	
	SWITCH,TOGGLE	911000048	15605	8280K16	1	
	SWITCH,TOGGLE	911000049	15605	7586K6	1	
	SWITCH,TOGGLE	911000050	15605	8363K7	9	
	SWITCH,TOGGLE	911000051	15605	8282K14	3	
	SWITCH,ROTARY	911200176	76854	01-083-02-07-4	1	
	SWITCH,PUSHBUTTON	911300031	C4426	76-2356/403	1	
	SWITCH,PUSHBUTTON	911300032	76854	57-41682-36	1	
	LAMP	913800046	07397	30934-0	13	
	LENS,WHITE	913800047	07397	30146-0	8	
	LENS,BLUE	913800048	07397	30143-0	2	
	LENS,RED	913800049	07397	30142-0	2	
	LENS,AMBER	913800050	07397	30140-0	1	
	SOCKET	913800051	07397	30097-0	13	
	JACK,TEST POINT,WHITE	914400025	98291	SKT-10	5	
	BINDING POST,MINEATURE,RED	915200017	58474	CF21RC	4	
	BINDING POST,MINEATURE,BLACK	915200018	58474	CF21BC	1	
	KNOB	916000110	49956	50-1WD-1G	3	
	KNOB,CONCENTRIC,ROUND,LOWER	916000111	49956	70-KB-2G	1	
	KNOB,DIAL SKIRTED, BAR	916000112	49956	70B-3-2G	12	
	POWER CORD	916400033	70903	17409	1	
	HANDLE	918100035	94668	B02692900	2	
	MATRIX ASSEMBLY	919900044	94668	C02651700	1	
	INTERFACE SELECTOR SWITCH ASSEMBLY	919900045	94668	C02691600	1	
S9	SWITCH ASSEMBLY	C02650500	94668	C02650500	1	
S11	SWITCH ASSEMBLY	C02650600	94668	C02650600	1	
S13	SWITCH ASSEMBLY	B02650700	94668	B02650700	1	
S14	SWITCH ASSEMBLY	B02650800	94668	B02650800	1	
S16	SWITCH ASSEMBLY	C02650900	94668	C02650900	1	
S17	SWITCH ASSEMBLY	B02651000	94668	B02651000	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
S19	SWITCH ASSEMBLY	C02692400	94668	C02692400	1	
S20	SWITCH ASSEMBLY S20	B02692800	94668	B02692800	1	
S21	SWITCH ASSEMBLY	B02651300	94668	B02651300	1	
S22	SWITCH ASSEMBLY	B02651400	94668	B02651400	1	
S23	SWITCH ASSEMBLY	C02651500	94668	C02651500	1	
	SWITCH ASSEMBLY	B02650700	94668	B02650700		
	SWITCH,ROTARY	911200179	76854	C1-C82-03-07-4	1	
	SWITCH ASSEMBLY	B02650800	94668	B02650800		
	SWITCH,ROTARY	911200178	76854	C1-C81-06-07-4	1	
	SWITCH ASSEMBLY	B02651000	94668	B02651000		
	SWITCH,ROTARY	911200177	76854	C1-C82-03-07-4	1	
	SWITCH ASSEMBLY	B02651300	94668	B02651300		
	SWITCH,ROTARY	911200191	76854	C1-999-00-07-4	1	
	SWITCH ASSEMBLY	B02651400	94668	B02651400		
	SWITCH,ROTARY	911200182	76854	C1-C82-05-07-4	1	
	SWITCH ASSEMBLY S2C	B02692800	94668	B02692800		
	SWITCH,ROTARY	911200181	76854	C1-C82-04-07-4	1	
	SWITCH ASSEMBLY	C02650500	94668	C02650500		
	SWITCH,ROTARY	911200175	76854	C1-C81-00-07-4	1	
CR1	DIODE	910600011	C7263	1N959B	1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
	SWITCH ASSEMBLY	C02650600	94668	C02650600		
	SWITCH,ROTARY	911200180	76854	C1-C80-00-07-4	1	
	SWITCH ASSEMBLY	C0265090C	94668	C02650900		
	SWITCH,ROTARY	911200190	76854	C1-999-00-07-4	1	
	SWITCH ASSEMBLY	C02651500	94668	C02651500		
	RESISTOR,FXD,WW,397OHMS,C.1W,PERM 1 PCT AXIAL LEADS	906100145	17870	1402	1	
	SWITCH,ROTARY	911200183	76854	C1-081-11-07-4	1	
	SWITCH ASSEMBLY	C02692400	94668	C02692400		
	SWITCH,ROTARY	911200174	76854	267-943-GK2	1	
R1	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R2	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R3	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R4	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R5	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R6	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R7	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R8	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R9	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R10	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R11	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R12	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R13	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R14	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	
R15	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R16	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	C1121		1	
R17	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PERM 5 PCT	906900304	01121		1	

REF DESIG	DESCRIPTION	SIERRA PART NUMBER	FMC	DRAWING NO. OR MFG NO.	QTY	EFFECTIVITY CODE
R18	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R19	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R20	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R21	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R22	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R23	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R24	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
R25	RESISTOR,FXD,COMPOSITION,30CKOHMS,1/4W, PORM 5 PCT	906900304	01121		1	
	FRONT PANEL	D02647001	94668	D02647001		
	PANEL,BLANK	919700006	98376	Z720-296COL-5	1	

SIERRA OFFICES

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